COS DCE Memory Regions (for Memory Monitor purposes)

COS DCE Memory Monitors may select one of three regions: CODE space, External RAM (XDATA), or Internal RAM.

The first two regions are fairly clear-cut. Within the 8051, the CODE space and XDATA space are separate memory devices unless, by design, a common memory device is used. Both have an address range of 64KB (0000-FFFF). For the COS DCE, below the 16KB address, CODE and XDATA remain separate. CODE space holds the Boot code and XDATA holds various upload and download buffers as well as boot mode patchable constants. From the 16KB mark (4000h) through the 32KB mark (7FFFh), the COS DCE has hardware I/O space and should not be read for memory monitor purposes. Above the 32KB mark (8000h – FFFFh), CODE and XDATA are merged and so are indistinguishable.

The Internal RAM space is perhaps a little more confusing. The particular flight-hardened processor used by the COS DCE has not only the basic 256 bytes of internal RAM but also has an additional 128 bytes. Unfortunately, the internal RAM address range is only 00-FF. This conflict is resolved through the ability of the 8051 to read/write internal RAM via either direct or indirect addressing. The below memory map details the various regions:

Address	Memory Purpose (Method of Addressing)	
80 – FF	User RAM (Indirect)	SFR (Direct)
00 – 7F	User RAM (Direct or Indirect)	

"SFR" is the bank of Special Function Registers. These registers include the hardware ports, data pointer, accumulators, and registers controlling particular hardware within the processor.

The current implementation of Memory Monitors for internal RAM uses Indirect Addressing, thereby preventing the reading of the SFR bank.