FUV Detector System
Printed Wiring Assembly Qualification Status

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FUV Board Qualification Status

Center for Astrophysics and Space Astronomy

COS Flight Board Qualification Testing

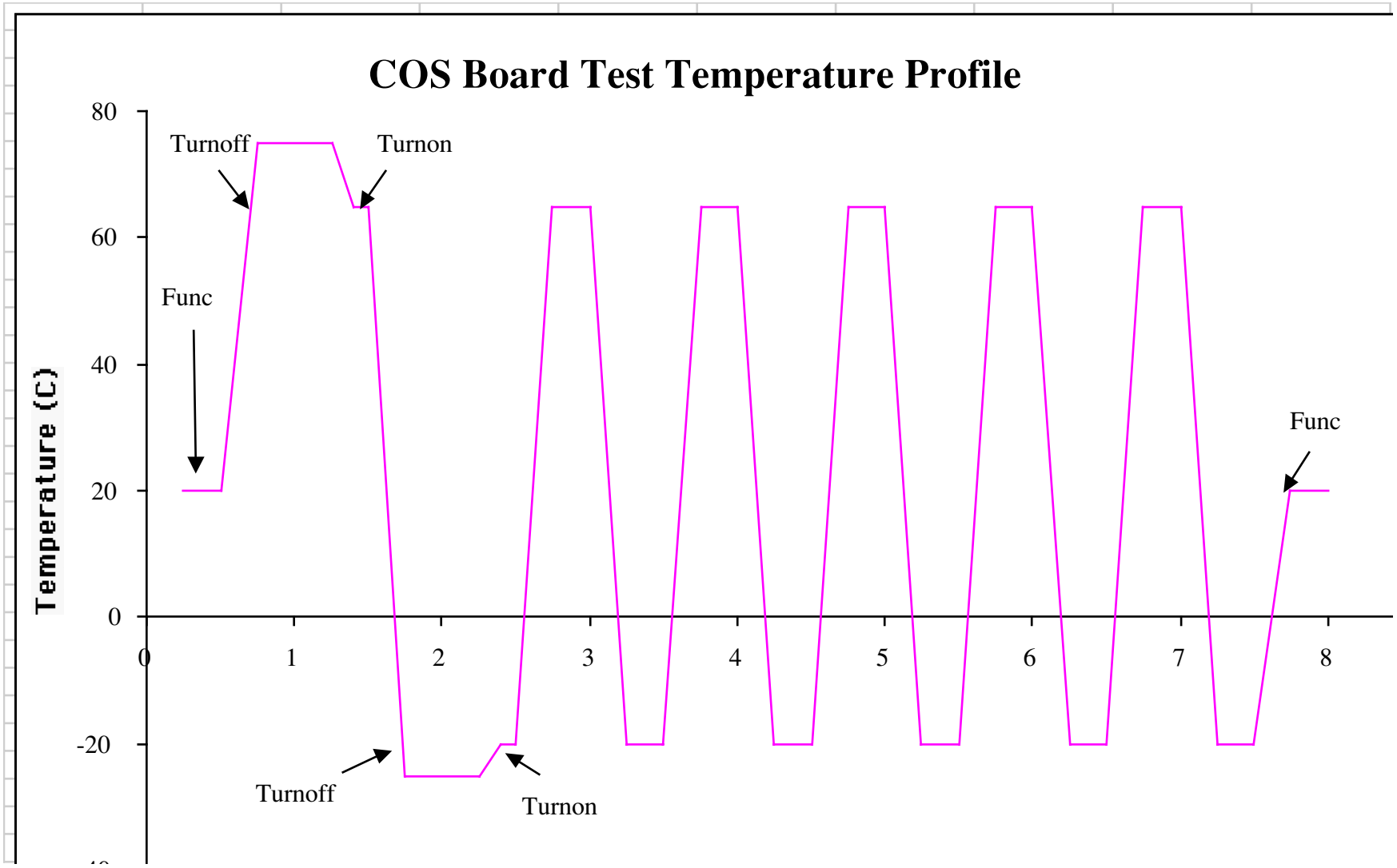
Unit	# of Units	# at a time	Process	Power?	High Temp	Low Temp	Duration	Status	Notes
LVPC	2	1	Hot Survival	N	75	N/A	1hr	Done	
	2	1	Turnon	Y	65	-40	N/A	Done	
	2	1	Hot Turnon	Y	65	N/A	N/A	Done	
HVPS	2	1	Hot Survival	N	75	N/A	1hr	Done	
	2	1	Cold Turnon	Y	N/A	-25	N/A	Done	
	2	1	Hot Turnon	Y	65	N/A	N/A	Done	
HVFM	2	1	Hot Survival	N	75	N/A	1hr	Done	
	2	1	Cold Turnon	Y	N/A	-25	N/A	Done	
	2	1	Hot Turnon	Y	65	N/A	N/A	Done	
Amplifier	1	1	Voltage Margin	Y	65	-20	N/A	Done	+/-7% of +5.5V Supply voltage
	4	4	Survival	N	75	-25	1hr each temp	Done	
	4	4	Turnon	Y	65	-20	N/A	Done	
	4	4	Thermal Cycle	Y	65	-20	6 cycles	Done	
	4	4	Soak/Burnin	Y	65	N/A	144hrs	Done	
DCE	1	1	Voltage Margin	Y	Ambient	Ambient	N/A	Done	+/-7% of 5V Supply voltage
	1	1	Freq Margin	Y	Ambient	Ambient	N/A	Done	+/-10% Frequency
	2	1	Survival	N	75	-25	1hr each temp	Done	
	2	1	Turnon	Y	65	-20	N/A	Done	
	2	1	Thermal Cycle	Y	65	-20	6 cycles	Done	
	2	1	Soak/Burnin	Y	65	N/A	144hrs		Or 1000hrs at ambient
TDC (XY pair)	1	1	Voltage Margin	Y	Ambient	Ambient	N/A	Done	+/-7% of Supply voltage
	1	1	Freq Margin	Y	Ambient	Ambient	N/A	Done	+/-10% Frequency
	4	1	Survival	N	75	-25	1hr each temp	In Prog	
	4	1	Turnon	Y	65	-20	N/A		
	4	1	Thermal Cycle	Y	65	-20	6 cycles		
	4	2	Soak/Burnin	Y	65	N/A	144hrs		Or 1000hrs at ambient

FUV Subassembly Run Time as of 11/1/2000

Reported in hours

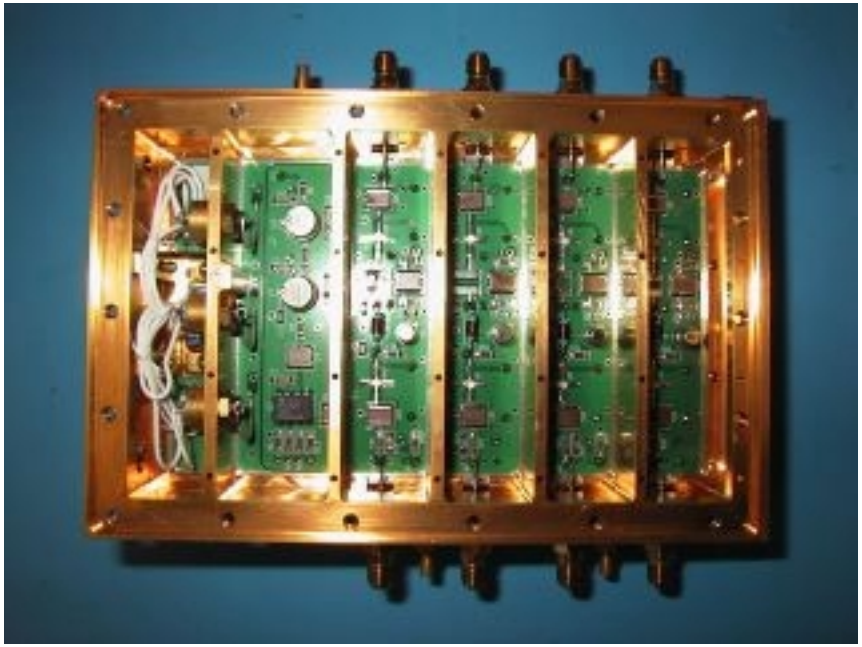
Subassembly	Set 1	Set 2
Amplifiers	1026	985
DCE	807	728
LVPC	437	6
TDCs	232	1
HVPS	175	1
HVFM	6	1

FUV Electronics Board Temperature Profile



Amplifier Functional Test Summary

Amplifier Functional Test Procedure COS-UCB-PRO-1093



- Static Tests (resistances)
- Current measurements
- Pulses of varying amplitude applied to each input
- Scope traces captured on each of the four outputs
- Output pulses characterized for timing amplitude, charge amplitude, and pulse width
- Charge output characterized vs. input
- RMS noise of fast outputs
- RMS noise of charge outputs

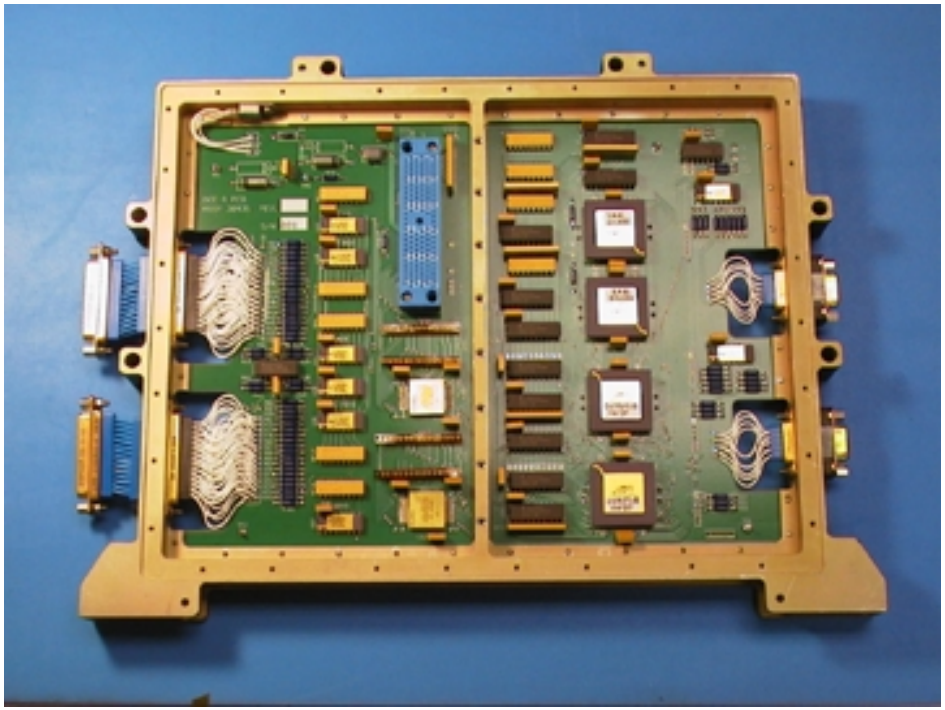
Amplifier Qualification Test Summary

- Amplifier Qualification Tests Performed (all four units):
  - Voltage Margin test at 5.115V and 5.885V
  - Hot Survival Soak, 2 hrs at 75C (unpowered)
  - Hot Turnon Test at 65C
  - Cold Survival Soak, 2 hrs at -25C (unpowered)
  - Cold Turnon Test at -20C
  - 5 Additional cycles between -20C and 65C
  - Powered Hot Soak at 65C for 696 hrs total (two separate soaks)

Amplifier Test Results/Issues

- Amplifiers perform in all test environments:
  - <4.5ns FWHM fast output pulse width exceeds specification of 5ns max in all environments
  - Max RMS noise for fast output is met with 1.5mV max for all amp units
- Closeouts
  - Waiver for de-rating of filter feedthru capacitor is pending approval

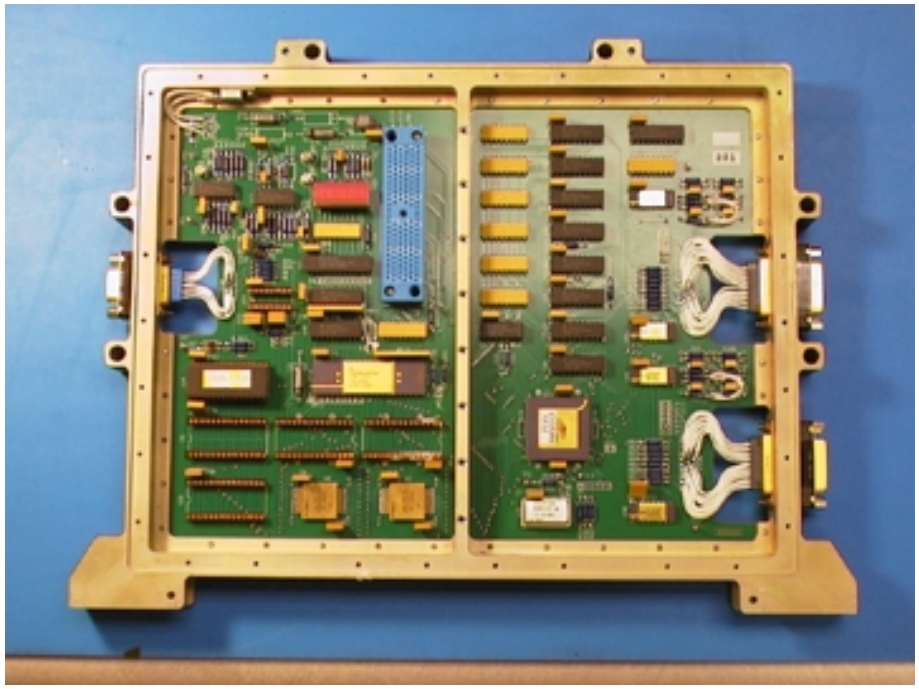
DCE-A Functional Test Procedure COS-UCB-PRO-1113A



- Static Tests (resistances)
- Current measurements
- Verify all Counter and Round-Robin ACTEL functions
- Verify Pulse-Height-Histogramming function
- Verify Science Data communications channels
- Characterize science data event loss under burst conditions
  - Segment A, Segment B, Both
- Verify no corruption of science data under burst conditions

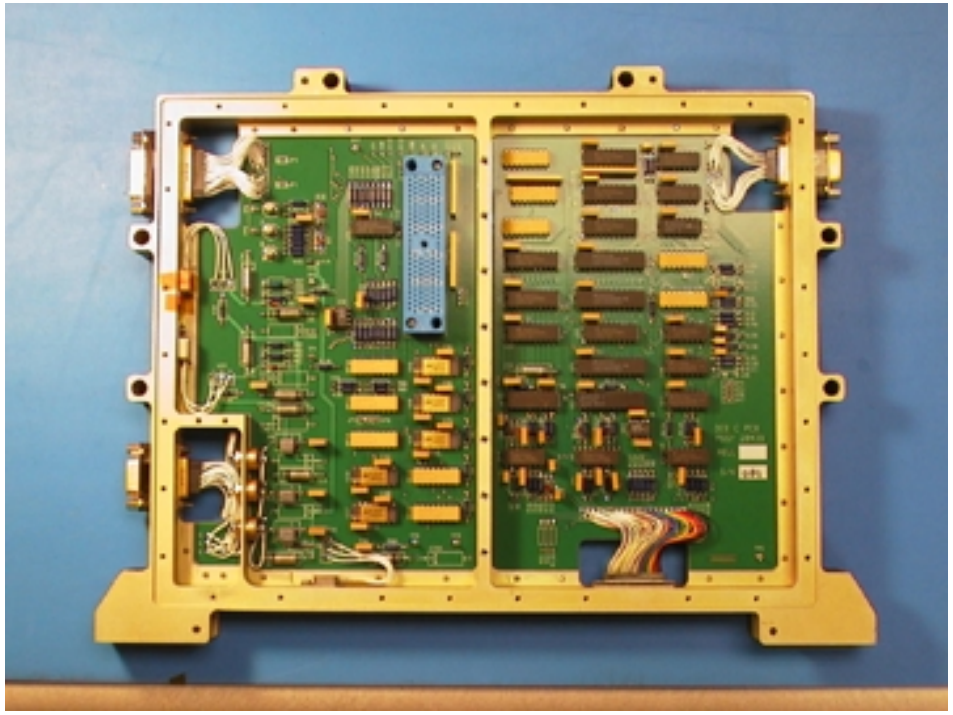
DCE-B Functional Test Summary

DCE-B Functional Test Procedure COS-UCB-PRO-1109



- Static Tests (resistances)
- Current measurements
- Verify CPU ACTEL functions
- Verify Command and Housekeeping communications Channels
- Verify Address decoding
- Verify control of DCE-A and DCE-C board functions

DCE-C Functional Test Procedure COS-UCB-PRO-1124A



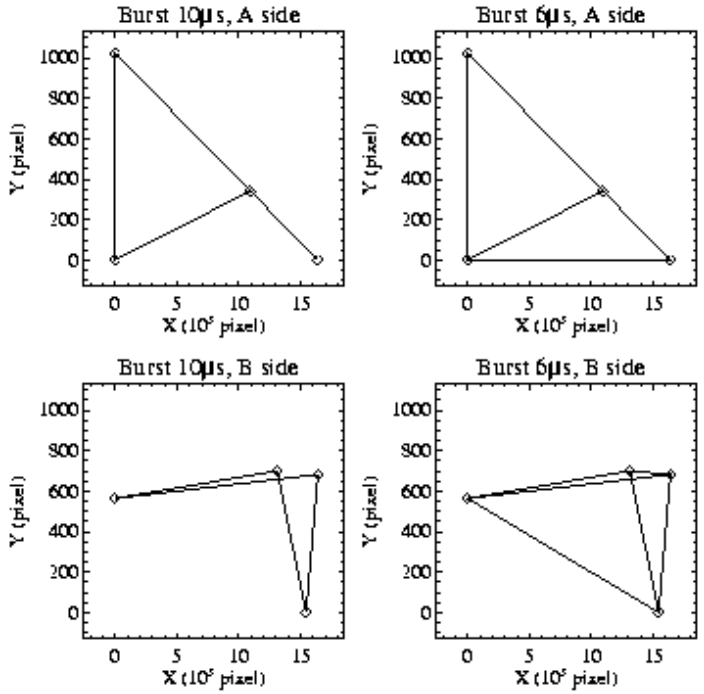
- Static Tests (resistances)
- Current measurements
- Verify High Voltage command logic
- Verify collection and reporting of analog housekeeping
- Verify bi-level command registers and talkbacks

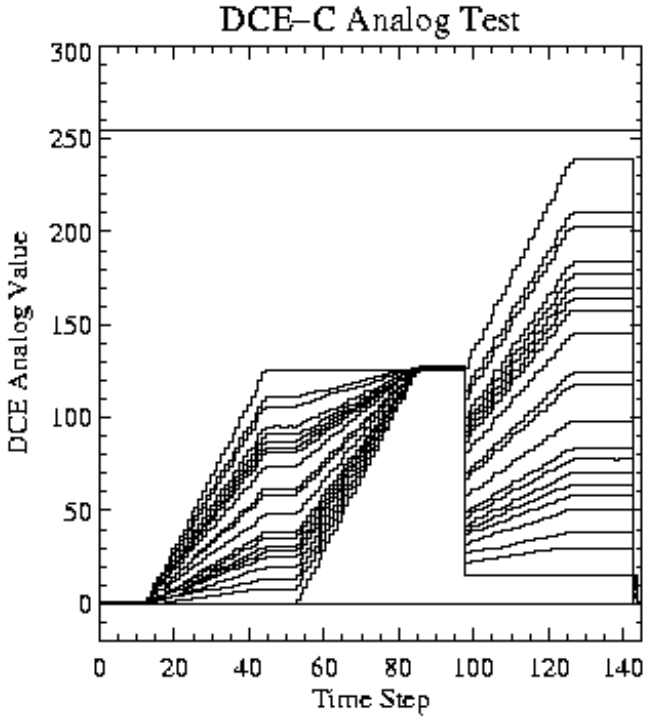
DCE Qualification Test Summary

- DCE Qualification Tests Performed:
  - Voltage Margin test at 4.65V and 5.35V
  - Frequency Margin test from 14.4MHz to 17.6MHz
  - Hot Survival Soak, 2 hrs at 75C (unpowered)
  - Hot Turnon Test at 65C
  - Cold Survival Soak, 2 hrs at -25C (unpowered)
  - Cold Turnon Test at -20C
  - 5 Additional cycles between -20C and 65C

DCE Test Results

- DCEs perform over all environments tested:
  - Science data uncorrupted, data rates exceed specification
  - Processor and memories functioned without incident in all cases
  - Housekeeping analogs steady



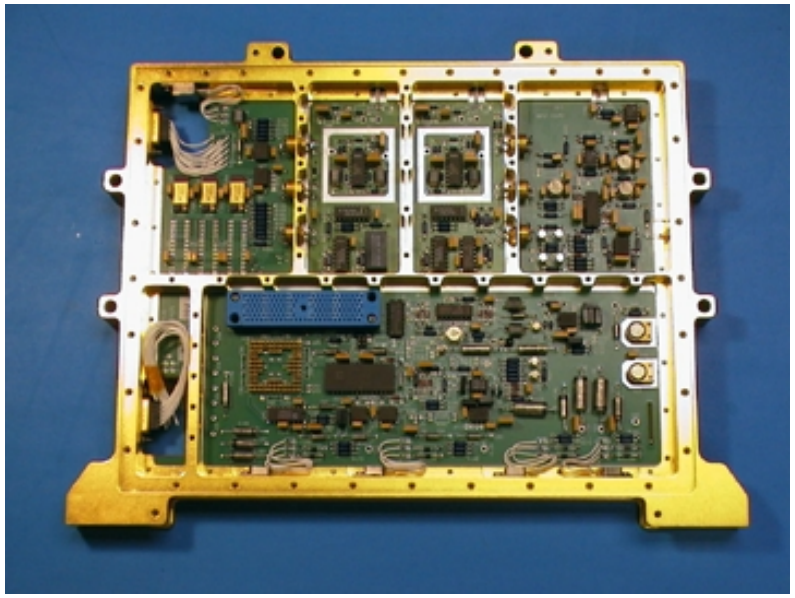


DCE Issues/Closeouts

- Issues
  - The redundant Command and Housekeeping channel ("B" side) was not handling housekeeping properly. PFR#007 was filed, and DCE testing continued on the "A" side. It was determined shortly thereafter that there was an incompatibility between the new BOOT code and OPERATE. A fix was applied to OPERATE, was verified, and the PFR closed.
  - After completion of the second DCE board qualification, several enhancements to the Power-On-Reset circuit were suggested by J&T. UCB agrees that the enhancements are a good idea, and would improve the robustness of the circuit.
- Closeouts
  - Apply minor enhancements suggested by J&T. This can be done with minimal impact if folded in with qualification of the TDC boards. Changes described in EC#0051.

TDC Functional Test Summary

TDC Functional Test Procedure COS-UCB-PRO-1121



- Static Tests (resistances)
- Current measurements
- Measure State Machine clocks
- Verify, Characterize stim function
- Verify TDC Data interface
- Verify commanded and power-on-resets
- Verify TDC commanding, DACs, and MUXs
- Measure imaging linearity
- Verify characterize charge thresholds
- Measure imaging resolution

TDC Qualification Test Summary

- TDC Qualification Tests Performed:
  - Voltage Margin test (one unit)
    - Vcc= +4.65V to +5.35V
    - Vee=-4.85V to -5.55V
    - "+15V" = +13.5V to +16.5V
    - "-15V" = -13.5V to -16.5V
  - Frequency Margin test (one unit only)
    - ISM Clock Period = 342ns to 274ns
    - OSM Clock Period = 305ns to 180ns
- TDC Qualification Tests to be Performed:
  - Hot Survival Soak, 2 hrs at 75C (unpowered)
  - Hot Turnon Test at 65C
  - Cold Survival Soak, 2 hrs at -25C (unpowered)
  - Cold Turnon Test at -20C
  - 5 Additional cycles between -20C and 65C

TDC Test Results/Issues

- Preliminary result: TDCs pass voltage and frequency margin testing
  - Data reduction in progress
- TDC's give excellent results with flight detector, see McPhate presentation
- TDC Actels not yet officially approved, in review. TDC testing is underway with a single pair of flight Actels.

Contamination Control Measures

- All FUV hardware (DVA & DEB) cleanliness requirements outlined in COS Cleanliness & Contamination Control Plan (IN0090-111)
- Materials selection conforms to RP 1124 & GSFC materials selection guide (TML< 1%, CVCM < 0.1%)
- Mechanical Parts:
  - All metal piece parts precision solvent cleaned per UCB-COS-PRO-1008
  - Door motor assemblies have been disassembled, solvent cleaned, and vacuum baked. Motors assembled into Drive Unit and certified with a TQCM at CASA
- Electrical
  - Cables: solvent cleaned under a black lamp then vacuum baked at 90C, and "tube" bagged for handling and test prior to delivery. Harnesses will be cleaned again with a clean room vacuum under UV black lamp.

Contamination Control Measures (cont)

Item Stage	Requirements	Tests Performed	Procedures
PC Board	Certifications, PCB Bake (for 12 hrs @ 80C); Start Sub-Assembly Unit File (Schematic, Parts List, EE Assembly Procedure)	Coupon Test, Visual Inspection	Goddard Space Flight Center (GSFC) Test of PCB Coupons
PCB Population	Parts Kits, E-Box Unit File	Workmanship QA Inspection	NASA-STD-8739.X
Sub-Assembly: Electronic Assembly (Frame)	Mechanical Drawing, Torque value list, Mechanical Assembly Procedure, Sub-Assembly Unit File	Visual Inspection	Document Results
Electronic Functional Test of PCB	Test Procedure, Sub-Assembly Unit File	Electronic Functional Test of Individual E-Box Unit	Document Results
Voltage Margin Test	Board or Sub-Assembly Level Test Procedure, Sub-Assembly Unit File	+65C to -25C, Regulated Supply 1% Accuracy	Test at Both Temp Extremes +/- 7% Supply Voltage, Document Results
Trim Set	Trim Set Documentation, Sub-Assembly Unit File	Electronic Functional Test of Individual E-Box Unit	
Thermal Cycle DRY (non-vacuum)	Sub-Assembly Level Test, Sub-Assembly Unit File	6 to 12 cycles, 2C per minute, for 96 hrs. Soak for two (2) hours at each extreme	-20C to 65C
Thermal Soak ACTIVE (vacuum or non-vacuum)	Sub-Assembly Level Test, Sub-Assembly Unit File	Vacuum : +65C max for 144 hrs., -25C min for 24 hrs. Non Vacuum : +80C max for 144 hrs, -25C min for 24 hrs	If no Thermal Vac
Alcohol Spray, Vapor Degrease	Cleaning and Degreasing Procedure, Sub-Assembly Unit File	Visual Inspection	Document Results
Staking, Coating	Staking and Coating Procedure, Sub-Assembly Unit File	Visual Inspection (Day- and UV Light Source)	MPD-313-008 GSFC
Component Assembly	Start Component Assembly File, Mech. Assembly Drawing, Electrical Cable Drawing	Visual Inspection	QA Inspection by GSFC
Formal Verification Testing (Component Level)	Verification Test Procedure, Component Assembly File	Verification Test	Document Results
Thermal Vacuum Bake	Test Procedure, Component Assembly File		
Vibration	Vibration Test (Outsourced) Documents, Component Assembly File	Vibration Test	Vibration Test Approval by GSFC
Component Cleaning	Cleaning and Degreasing Procedure	Visual Inspection	
Sub-System : EMI/EMC	Test Procedure, Component Assembly File	EMI/EMC	
Thermal Vacuum (Sub-System Level)	DDL Vacuum Assembly (DVA) and Detector Electronics Box (DEB), Component Assembly File	Subsystem Thermal Vac - 6 cycles, Total Duration 96 hrs (operational); All Mechanisms Operated at Specified Extremes (one hot and one cold start required).	See Thermal Vacuum Procedures (+65C for 144 hrs, -25C for 24 hrs)
Ship (Sub-System Level)	Component Assembly File		
Thermal Balance (Sub-System Level)		Performed at Ball Aero Space (BASD)	
Note: All assembly work requires a ESD-safe assembly area. All actions performed are documented and added to the individual E-Box unit's file or the flight system's E-Box .			

Unit Cleanliness Processing

Unit Cleanliness Processing Matrix							as of 11/4/00		
Process	Amps	HVFMs	LVPCs	HVPSs	TDCs	DCEs	Harness	Motor	
Vacuum Bake	T	X	X	X	T	T	X	X	
TQCMmeasure		X	X	X				X	
Precision Clean	X	X	X	X	T	T		X	
Vapor Degrease	X				T	T			
Conformal Coat	X	X	X	X	T	T			
Air Bake	X	X	X	X	T	T			
Solvent wipe							X		
Blacklight Clean	T	T	T	T	T	T	X		
X - Work Performed				T - Work to be Performed					

Power System Cleanliness Processing

- HVFMs do not degrade system resolution (test UCB-COS-PRO-1085)
- HVFMs Rough vacuum baked to 60C (10^{-2} Torr)
  - 76 hrs for unit 1 and 162 hrs for unit 2
- HVFMs, LVPCs, and HVPSs high vacuum baked together at 60C (4e-5Torr) for 144 hrs, all six units
- TQCM measurements give an OGR of 1.43e-14 gm/cm^2/s
  - Exceeds COS spec of 4.3e-13 gm/cm^2/s
  - Measurements made prior to conformal coating, and were for early detection of any EN-11 potting outgassing problems, not to certify these components. Certification occurs at system level.
- TQCM measurements and calculations recorded in UCB-COS-PRO-1103
- HVFMs precision cleaned, conformal coated, and air-cured 24 hrs 60C.
- 1 LVPC and 1 HVPS cleaned and conformal coated.
- Remaining electronics to be conformal coated, cured and vacuum baked.

Electrical Harness Cleanliness Processing

- Flight harnesses built clean
- Rung out by independent technician
- Solvent wiped with Isopropyl Alcohol
- Blacklight inspected and cleaned
- Vacuum baked at 90C for 72 hours
- Harness bagged for lab environment prior to ship
- Bagging removed prior to final pre-ship blacklight inspection