HST/COS FUV Detector Operations Manual

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1. INTRODUCTION

The purpose of this document is to provide a detailed description of how to operate the Hubble Space Telescope / Cosmic Origins Spectrograph (HST/COS) far ultraviolet (FUV) detector under normal laboratory level conditions. This document contains information relevant to operating the FUV detector from the electronic ground support equipment (EGSE). The purpose is to give the generic detector operator a systems level understanding of the detector hardware and software and specific instructions on how to operate the detector safely in a variety of operational situations. This document provides a general overview of the detector and EGSE hardware along with pertinent design information regarding the EGSE and flight software. Finally, detailed instructions are provided including a comprehensive listing of all detector commands, functions, and procedures needed to safely operate and control the FUV detector.

1.1 FUV DETECTOR OVERVIEW

The FUV detector subsystem is a dual channel photon-counting detector that converts light focussed on its photosensitive front surface into a stream of digitized photon coordinates. The FUV detector subsystem consists of two major components, the Detector Vacuum Assembly (DVA) and the Detector Electronics Box (DEB), interconnected by ~2m long power, data, signal, and high voltage lines. The DVA performs the conversion of light to analog electronic impulses and is located on the optics bench in the COS instrument. The DEB converts the 5 analog signals per segment from the DVA into digitized coordinates and is located on the thermal shelf within the COS enclosure. The DEB also manages the power. A functional block diagram of the FUV detector system is shown in Figure 1.1-1.

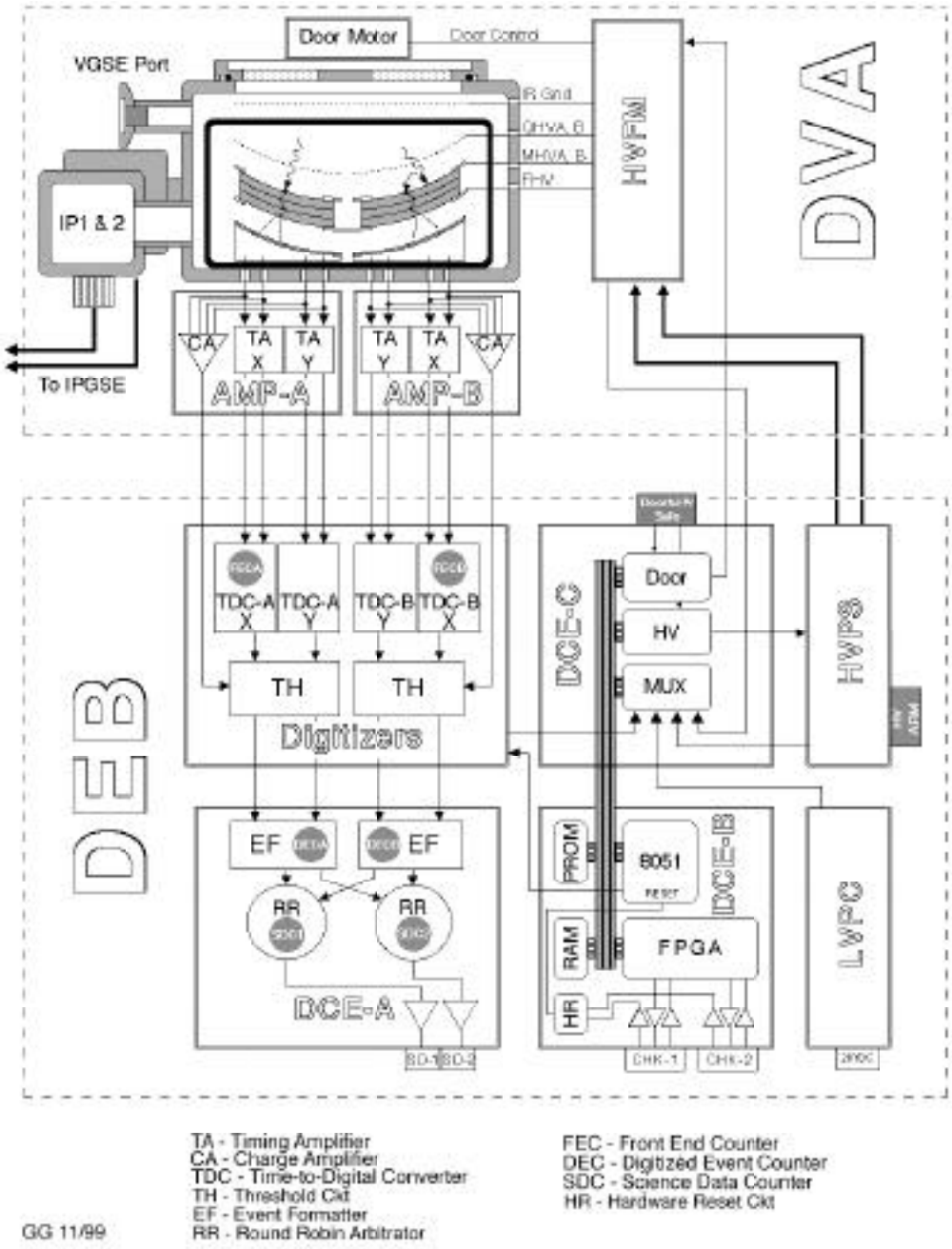


Figure 1.1-1: Functional schematic of the FUV detector system.

1.1.1 The Detector Vacuum Assembly

The detector vacuum assembly (DVA) consists of the detector backplate assembly (DBA) and the vacuum housing assembly (VHA). The DBA consists of the detector backplate, anode assembly, brazed body assembly (BBA), the high voltage filter module (HVFM), and the amplifier assembly. The BBA houses the microchannel plates and the QE enhancement grid. The VHA consists of the vacuum box, door assembly, door motor, and ion pumps. The DVA produces 5 analog signals for each detected event that are passed to the DEB, i.e., 2 timing signal pulses for each x and y and 1 charge signal per event.

The active front surface of the detector is curved to match the design focal surface radius of curvature of 826 mm. To achieve the length required to capture the entire projected COS spectrum, two detector segments are placed side by side with a small gap between them. To mitigate risk of single-point-failure, the two detector segments are

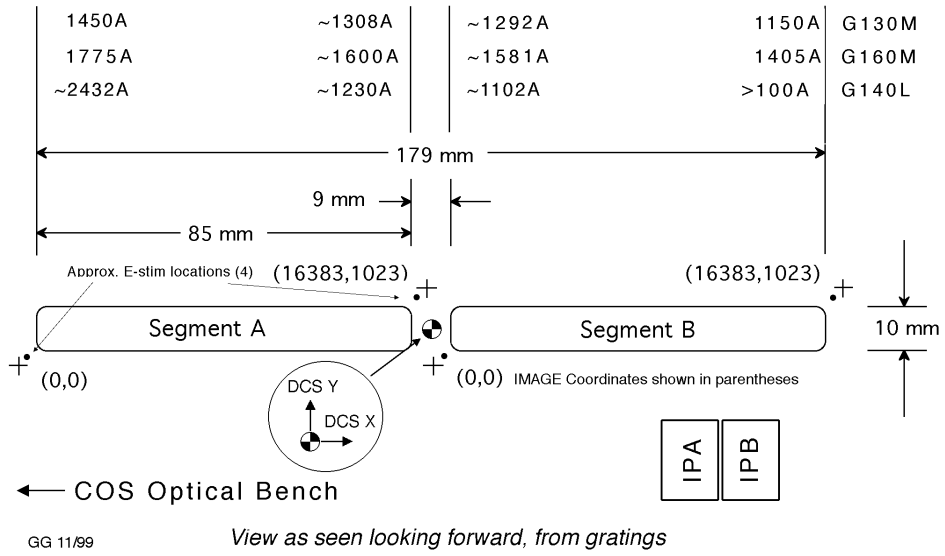


Figure 1.1-2: Active area of the FUV detector and relative alignment of each segment.

independently operable: loss of one segment does not compromise the independent operation of the other. Each detector segment has an active area of 85 x 10 mm digitized within a 16384 x 1024 pixel digital region as shown in Figure 1.1-2.

The detector door mechanism provides a means of maintaining high vacuum from final assembly through launch. The door mechanism mounts to the top of the vacuum housing

and is essentially a gate valve that seals the detector aperture of approximately 200 x 20 mm. UV transmissive windows are mounted in the door frame, above each detector segment, to permit ultraviolet stimulation of small portions of the detector while the door is closed. During thermal vacuum testing, the door will be opened and closed; however, once in orbit, the door is activated once and remains open for the duration of the mission. The door is driven by a brushed DC gear-motor and gearbox. The door may also be opened by a redundant spring release mechanism activated by a wax actuator. The wax actuator has redundant heater windings. The spring release mechanism can be reset with an operating door motor.

The high voltage filter module (HVFM) is mounted to the back of the DVA and takes raw high voltage from the high voltage power supply (HVPS) in the DEB and produces the five HV levels required by the MCP stack. These are the field high voltage (FHV), the microchannel plate high voltages (MHVA and MHVB), and the QE enhancement grid high voltages (QHVA and QHVB). The HVFM also filters the MHVA and MHVB to suppress noise and high voltage oscillation.

Also mounted to the back of the DVA are the two amplifier units, one for each segment of the detector. These amplifiers take the 4 charge pulses from the cross-delay line anode (2 for x and 2 for y per detector segment) and convert them to 5 analog voltage pulses (4 timing and 1 charge) that are then fed to the time-to-digital converters (TDC) in the DEB.

1.1.2 The Detector Electronics Box (DEB)

The DEB is comprised of the high voltage power supply (HVPS), the low voltage power converter (LVPC), the time-to-digital converters (TDCs), and the detector control electronics (DCE-A, B, & C).

The HVPS produces one commandable high voltage output for each of the two detector segments (2.5-6.5kV). These two high voltages connect to the High Voltage Filter Module on the Detector Vacuum Assembly.

The LVPC converts the nominal +28 volt input from the spacecraft power bus into numerous low-noise and ground-isolated voltage outputs used by the various components of the FUV detector subsystem. +/- 15V for the HVPS and HVFM, +28V for the HVPS, +5 and +/-15V for the amplifier units and TDCs, and +5 and +/-15V for the DCE are all provided as secondary outputs. All outputs are post-regulated at the point of use. A current-limited two-fault tolerant +28V switched output is also provided, to service the various auxiliary functions required by the FUV detector subsystem. These functions include reversible motor drive for the detector door and redundant actuator power.

The TDCs process the amplified anode timing signals from the DVA to calculate photon position coordinates. In addition, each TDC contains a circuit which produces two alternating, periodic, negative polarity, tailed pulses which are capacitively coupled to both ends of the delay line anode. When active these electronic stims (e-stims or stim pulses) emulate counts located at the edges of the anode, beyond the illuminated regions of the detector (see Figure 1.1-2). The e-stims are useful as they provide a means of testing the functionality of the conversion and encoding electronics without applying high voltage to the detector. They also provide a metric for measuring, and thus correcting, drifts and shifts in the digitized photon locations due to thermal affects. Finally, the e-stims can be used as an alternate method for calculating the detector electronics dead time.

The DCE manages all of the communications, commanding, housekeeping, and autonomous operation of the detector system. Its functions are divided among three boards: DCE-A, B, and C.

- DCE-A filters the event stream and combines two streams into one. The event stream drives a RS422 3-wire interface referred to as Science Data. No Science Data appear in housekeeping.
- DCE-B is the command/housekeeping interface board and provides software control of the other boards. The board includes PROM for storing executable code, RAM from which code executes and data are stored, an 8051 microcontroller that executes the code, and RS422 hardware to support command/housekeeping.
- DCE-C provides door control, high voltage (HV) control, and analog-to-digital conversion for sensors.

1.2 DCE FLIGHT SOFTWARE

See section 8 for an overview of the DCE flight software.

2. SAFETY AND HAZARDS

2.1 HARDWARE SAFETY

2.1.1 Pressure Requirements

The FUV detector is an open face MCP detector. As such, it can be hazardous to the health and safety of the detector to operate the MCP HV if the vacuum at the MCPs is higher than $1X10^{-5}$ Torr. In addition, if the MCPs are exposed to air, preflight

conditioning of the MCPs will be lost and will require at least 1 month of reconditioning. For this reason, the detector is equipped with a door atop the DVA. The door shall be opened only when the DVA is in a vacuum tank and the vacuum readings from the ion pump indicate adequate vacuum has been achieved. Additionally, safe operation of the FUV detector's HV systems requires the that the ambient pressure environment of the FUV detector system be 500 Torr<P<$1X10^{-4}$ Torr. For pressures between $1X10^{-4}$ and 500 Torr coronal discharge can occur when high voltage is present, so all HV systems must be shut off when the ambient pressure is within this pressure regime. Once in a safe ambient vacuum environment, it is only safe to activate the FUV detector's HV after a vacuum of <$1X10^{-5}$ Torr inside the DVA has been achieved as measured by the flight ion pumps.

2.1.2 Detector Door

The detector door shall only be opened when the detector system is under vacuum and the ambient pressure is less than $1X10^{-5}$ Torr. The door subsystem has an safetly interlock system to minimize the chance that the door can be opened at an inappropriate time. For the door to operate the red safety plug on the front of the GSE must be removed. If the safety plug is installed then the door will not open. Under normal operating conditions on the ground the door shall not be operated! The door safe plug is accessable on the DEB and or on the front of the COS EGSE Interface Box, depending upon how the system is configured.

2.1.3 High Voltage Operation

The HV system is also interlocked at the DEB or through the front of the COS EGSE in a manner identical to the door interlock.. For HV to operate the HV safe plug must be removed.

2.1.4 Autonomous Protection Functions

The detector has two built-in software functions that provide autonomous action to protect the microchannel plates. These are HV overcurrent protection and count rate protection.

2.1.4.1 HV Overcurrent Protection

The current limit protection task checks the HV and Aux current readings for over-limit conditions. It reads the current values, records the information as data samples, and determines if an over-limit condition occurred. This task runs as fast as possible to monitor the power current levels. It reads the analog-to-digital converter (ADC) for HV current and Aux current. It saves the samples in RAM so that they can be downloaded for analysis if necessary. This task is capable of reporting HV glitches without turning

off the HV. It is also capable of recognizing a sustained over-limit condition. If the current level remains out of limits for more than 20 msec (5 discrete, contiguous samples), the task powers off the HV and reports the over-limit event in housekeeping. If a single over-limit event is detected, this task reports a diagnostic. Subsequent over-limit samples are counted but no diagnostic is posted until the consecutive out-of-limits count is reached. The out-of-limits count is a patchable constant. If a power current value within limits is read, the consecutive out-of-limits counter is reset to zero. When the consecutive out-of-limits count is reached, this task turns off power to the HV supply. After a limit violation has occurred, there is no autonomous method for turning HV back on. Default parameters for the Current Limit Protection Task are loaded during power-on reset initialization. The parameters can then be modified via DCE commands.

2.1.4.2 Count Rate Protection

The DCE FSW creates a Global Rate Monitor by routinely comparing the number of photon events counted by the Fast Event Counter (FEC) during a commandable interval against a commandable rate limit. When the count rate exceeds the limit over a given interval, then the DCE FSW autonomously changes state to FUVHVLow. The DCE will remain in the FUVHVLow state until commanded to another state. This rate is usually chosen conservatively to be just above the maximum source count rate allowed. The FEC in the FUV detector is a non-paralyzable counter and is therefore ideal for use as a rate monitor. The Global Rate monitor not only protects against over-illumination, but also the SAA, low level coronal breakdown, field emission, etc. It also acts as a backup to the HV current monitor. So even though the detector could handle high global rates for longer than 1 second without much gain degradation, the 1 second response time must be maintained to protect the detector for unforeseen failure mechanisms. The countrate at which HV is set to HVLow should be set conservatively to be above the maximum allowable count rate for the detector. Rates much higher than the setpoint (currently set at 20,000 cts/sec per segment for ground testing) indicate a problem, either internal to the detector or due to an operational error (e.g., failure to turn HV down for SAA) and the detector HV is set to FUVHVLow. The Global Rate monitor algorithm in the DCE monitors the Fast Event Counter (FEC) which is the counter on the front end of the TDC electronics that counts every event detected (whether "valid" or not) without respect to x,y position on the detector. This counter is read out every second. The shutdown algorithm can be summarized in the following way: Three parameters are used in the algorithm, trigger count C, integration time T, and samples N. At detector turn-on the flight software sets up rolling buffer of N elements. Each second the flight software populates an element of the rolling buffer with the FEC value for that segment and computes the average of all the values in the rolling buffer. If the average count rate exceeds C, then the detector HV is set to FUVHVLow. In other terms, the count rate protection algorithm compares a box car average against a preset value.

2.1.5 Thermal Runaway of Microchannel Plate Detectors

Thermal runaway is a major concern when operating a large format microchannel plate detector such as the HST/COS FUV detector. This concern is mitigated through cautious operational procedures which allow the microchannel plates to reach thermal equilibrium. For general user knowledge the following paragraphs outline the mechanism behind thermal runaway.

Thermal runaway is a condition experienced by microchannel plate (MCP) detectors, which can, if left unchecked, lead to complete destruction of the microchannel plates. The condition is brought about by two characteristics of microchannel plates, the low thermal conductivity of the MCP glass and the inverse relationship between the resistance of the glass and temperature. Starting with a MCP detector at room temperature, consider the top plate as isothermal with the edges in contact with the MCP housing. When the high voltage is turned on there is uniform current flow through the MCP as the resistance is uniform across the MCP. However, because the microchannel plate is resistive, power is dissipated in the microchannel plate, thus warming the microchannel plate. Now the problem becomes one of heat flow. As the MCP warms heat begins to flow out through the MCP to body interface. The heat flow is not very efficient given the poor thermal conductivity of the MCP glass, so a temperature differential forms with the geometric center of the MCP being the warmest. This thermal gradient leads to a resistive gradient, due to the inverse dependence on the resistance to temperature, with the center of the microchannel plate having the lowest resistance. This situation is, therefore, subject to a feedback loop, which causes the thermal runaway.

The feedback loops goes as follows. As the resistance drops the current flow, and thus the power dissipated in the microchannel plate, increases. As the power dissipated increases the resistance correspondingly drops, which leads to an increase in power and so on until the temperature at the center of the microchannel plates becomes so high that the glass actually melts and the detector is destroyed. Obviously the sensitivity of this feedback mechanism is completely dependent upon the exact nature of the MCP resistance versus temperature.

The conditions that lead to thermal runaway can be avoided through prudent start up procedures that minimize the likelihood of a thermal gradient, sufficient to initiate thermal runaway, from forming across the microchannel plate surface. Prudence is defined as allowing sufficient time during HV ramp up for the microchannel plates and detector body to thermalize, thus minimizing the potential of a strong thermal gradient across the microchannel plates.

At this time only experience and caution can be used as guides for determining the actual start up times needed to safely turn the detector on.

2.2 PERSONNEL SAFETY

The primary concern with respect to personnel safety is with the ion pump ground support equipment. The IPGSE employs a high power, high voltage power supply capable of supplying 5 mA of current at up to 5000 V. Before any IPGSE connections are handled all HV to the ion pumps must be turned off. Failure to do so constitutes a serious risk to the health and safety of the individual handling the hardware.

3. HARDWARE CONFIGURATIONS

3.1 DESCRIPTION OF THE ELECTRICAL GROUND SUPPORT EQUIPMENT

The electrical ground support equipment (EGSE) is the only means of controlling the detector. The EGSE consists of a shippable container with an internally shock mounted electronics rack that contains all of the support equipment necessary to operate the detector. The EGSE contains the following items (see Figure 3.1-1); a computer monitor, keyboard tray, COS EGSE Interface Box, computer controllable HP 6644 DC power supply, Sun SPARC computer, and APC 1400 uninterruptable power supply.

The computer display is for the SUN Workstation and is used to display detector status and the various windows necessary for control of the detector and analysis and display of the detector data. The keyboard tray holds the computer keyboard and spare cables for various and sundry things. The COS EGSE Interface Box is the intermediate box between the control computer and the detector DEC-B board. The HP 6440 power supply provides the +28V to the LPVC and is computer controlled. The SPARC station is the computer used to control everything. Finally, the APC 1400 is an uninterruptible power supply that can power the entire EGSE while the detector is shut down and put into a safe configuration. The APC 1400 is there to allow the operator to safe the detector in the event of power loss and shall not be used for extended detector operations.

The electrical connections between the COS EGSE Interface Box and the detector consists of four cables; one that provides power to the LVPC, one for command and housekeeping, one for science data, and one for SAFE plugs for the HV system and door. The details of the electrical connections are provided in the FUV Detector Interface Control Document (COS-UCB-001). It also provides access to the detector door and HV safe plugs as described in sections 2.1.2 and 2.1.3.

3.2 DESCRIPTION OF THE ION PUMP GROUND SUPPORT EQUIPMENT

The ion pumps on the DVA are only powered while on the ground and are inoperable in flight. An external pump controller is used to operate the ion pumps during all ground

testing. These external controllers are directly connected to the ion pumps through two HV cables. The internal pressure of the vacuum housing is registered on the ion pump

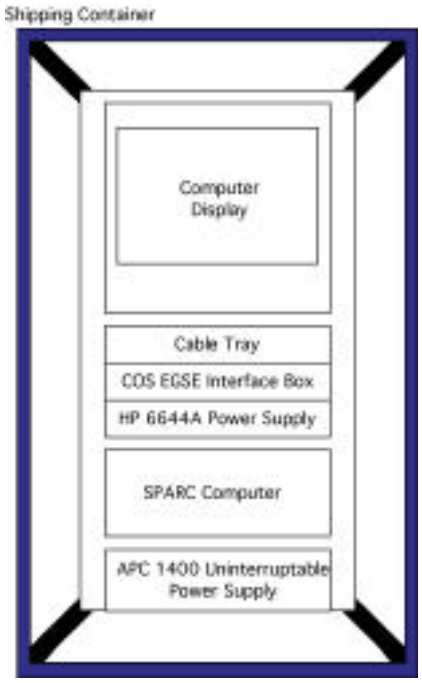


Figure 3.1-1: Schematic of the COS FUV detector electrical ground support equipment (EGSE).

controller directly and MUST be < 10^{-5} Torr for any MCP HV activities to conducted provide the previously stated environmental conditions are met.

4. EGSE SOFTWARE

The Electronic Ground Support Equipment (EGSE) software supports the operation of the FUV detector on the ground. The software system allows the user to send commands to the DCE and monitor the detector status in real time.

The EGSE software is run on the SUN workstation as described in section 3 when logged in as “eagcos”. This user account has a default login environment with all the needed paths set properly for running the EGSE software.

When starting a new session or set of tests, it is recommended to create and move to a new directory. Any new files created as the result of a command will be written to the

current directory. Before any commands are issued, a configuration file (Config) and a log file (Log) should be in this directory. The Config file contains information describing the current detector and system configuration and is manually updated by the operator. The Log file is used by the operator to manually enter information regarding the test or session in progress. Additionally, a Autolog file is automatically created and updated by the various commands when they are run. This allows the user to review the progress of the session at a later time.

The system is started with the procedure ***Pon*** (see section 5 for details). This procedure in turn calls a number of functions to put the detector system in a state ready to operate. The current state of the detector is described by the housekeeping which consists of a snapshot of the different parameters the FSW monitors (currents, voltages, temperatures, etc.).

4.1 SOFTWARE DESIGN / MEMORY MAP

The user starts the system by using the procedure Pon. This procedure configures the system and starts the processes costag, cmd_client, cmd_server and RTMON. These processes allow communication from the user to the detector DCE and vice versa. As part of the Pon procedure used to start up the system, a fixed size area of memory is allocated on the Sun workstation. The memory is divided in Housekeeping, Science Data, Command Data and Miscellaneous sections. These sections are shared by the different programs which allow communication and control of the detector. Figure 4.1.1 represents a high level diagram of the communication flow.

The cmd_client process receives instructions from the various commands entered by the user at the terminal window or through functions and procedures as detailed in section 5. This program then reads the string it received, interprets it and writes the corresponding executable code into the Command Data area of the shared memory. This area of memory can queue up to 8 commands.

When a command is written to the shared memory, the cmd_server process gets a signal (through threads) telling it that a command is waiting. This process then gets the reformated command from memory and passes it to the DCE via the EDT communication card. Once the command is read and sent to the DCE, the memory space it occupied is then cleared.

Every time the DCE receives a command, a new housekeeping packet is created and transferred to the appropriate section of the shared memory. This transfer is handled by the second EDT card through a configurable size I/O buffer and the costag process. The housekeeping only gets transferred to the costag process when the I/O buffer is full. This I/O buffer is also used to transfer science data from the DCE to the shared memory area.

The size of the buffer is a compromise between the rate of refresh of the housekeeping on the screen (smaller means more frequent updates) and the high transfer rate required for high rate science data acquisitions (bigger means higher transfer rate). The current size of the buffer makes for a housekeeping refresh rate of about once every second. The process costag then gets the data from the I/O buffer and writes it to the corresponding memory area (housekeeping or science). It also generates the pulse height histogram data and writes it to the miscellaneous area of shared memory. This data gets plotted on the screen at every refresh for each segment.

The user can view the status of the detector via the RTMON program which displays the "COS Real Time Housekeeping Monitor" window (described in section 4.2). This program gets a signal every time the housekeeping area gets updated, it then reads that section of the shared memory and updates the values on the screen. RTMON reads a file at startup with the different conversion factors for all the housekeeping items. This allows the program to convert the engineering values obtained from the DCE into meaningful units before displaying them on the screen (converting to volts, amps, degrees, etc.).

Additional programs also have access to the shared memory: sci2xyp reads the science data area and writes out a FITS file with events data as a binary extension table, sci2img creates an standard FITS file with an image as the primary data set. The program hklog reads the housekeeping memory area and writes its content as a FITS file providing a snapshot of the detector status. The program hkprint reads a user specified item in the housekeeping and is used in many of the commands described in section 5.

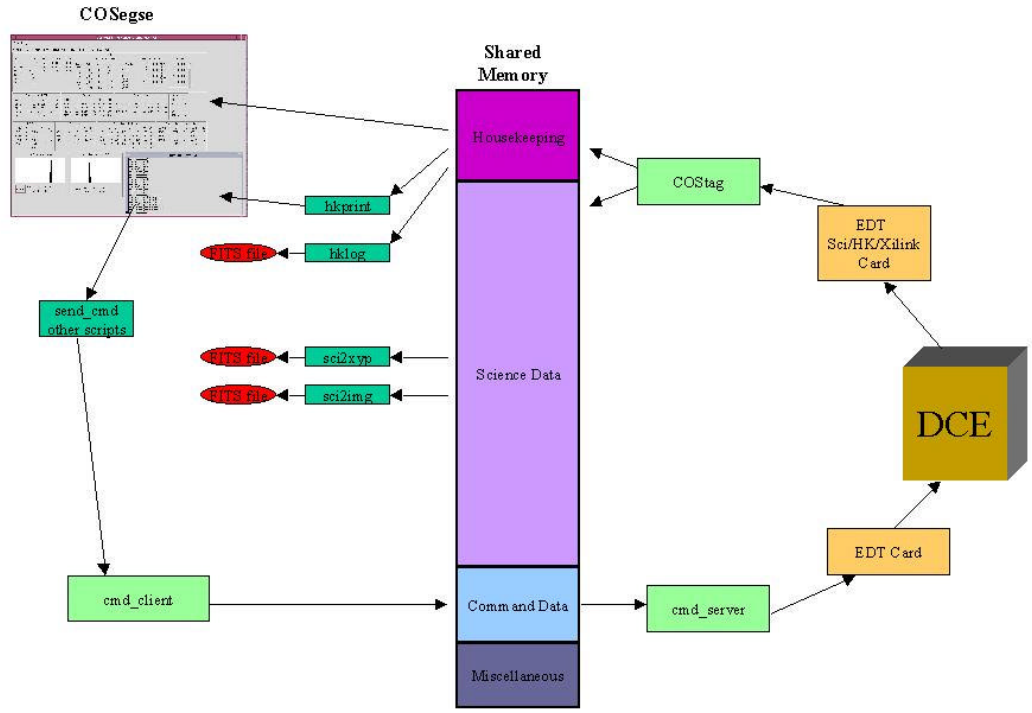
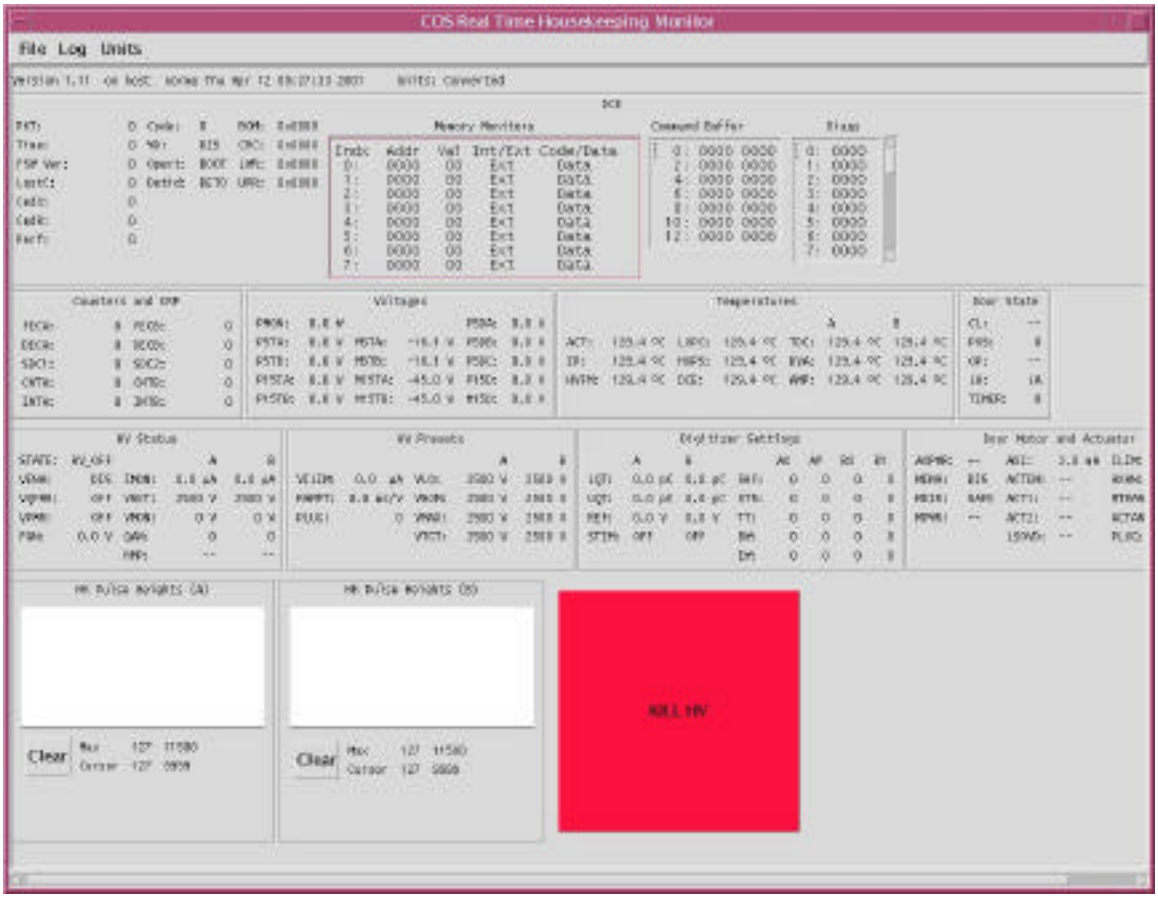


Figure 4.1.1: Functional schematic of the EGSE software.

4.2 MONITOR WINDOW



The monitor window is the only way to monitor the status of the FUV detector. It is run by the EGSE software as described above. In the following sections is a box-by-box description of each region, each monitor, and nominal ranges.

4.2.1 Upper left hand corner, unnamed area

Name	Description	Expected Value
PKT	Number of packets received, including no ops and housekeeping pkts being sent. Should be incrementing or you are frozen.	variable, increasing
Time	In units of DCE second, which is one second to within about 5%.	variable, increasing
FSWVer	Flight software version #.	1040

LastC	Last OpCode command executed	variable
CmdX CmdR	Number of commands executed. Number of commands received. These should be the same or there is/was a problem.	variable, increasing
Perf	Performance monitor. The performance monitor is an executive loop. The value here is basically how many background CRC regions (Cyclic Redundancy Check, which is a fancy check sum) you've gotten through since the last housekeeping packet. Higher number means less busy.	variable
WD	Watchdog reset circuit monitor. If the DCE FSW fails to service the watchdog within 10 seconds, the detector HV is turned off and the DCE FSW is forced to boot state.	0 = off 1 = on
Operat	Operate code. Whether the operate code is loaded.	0 = boot 1 = operate
Detid	Detector id	0 = ETU 1 = FUV01 (flight) 2 = FUV02 (spare)
ROM	PROM CRC. The last three digits will be c001 ("cool") when the operate code is loaded.	0xcoo1
CRC	Cyclic Redundancy Check. This value is always 0x0000 unless a commanded CRC is being done, then the value is 'code'. A CRC is commanded during the "Pon" sequence so the CRC will show "code" for a brief period of time during start up.	0x0000

4.2.2 Memory Monitors

The user defined memory monitor registers are set just after a code upload.

4.2.3 Command Buffer

Most recent commands issued, with parameter values and complements.
8080 is no-op command opcode
adad is upload command opcode

4.2.4 Diags

This box is for the diagnostic codes issued by the detector when an error is detected in the flight software. For each line in this box, the first two numbers of the value (nn in examples below) indicate the location within a 32 deep, push down stack (the locations range from 0 (top) to FF (bottom)); the second two numbers give the diagnostic as documented in the ICD. See section 6.1 of this document for a complete list of diagnostic errors. Some examples include…

nn1b = power-on reset
nn1c = watchdog reset
nn16 = HV current transient (above VILIM for at least one sample) from AUX
nn27 = HV current transient in segment A
nn28 = HV current transient in segment B
nn2a = autonomous HVI shut down segment A
nn2b = autonomous HVI shut down segment B
nn2e = autonomous shut down due to violation of the AUXI

4.2.5 Counters and CRP

This section is one of the sections an operator should routinely check as key health and safety information is displayed here.

ID	Description	Value
FECA FECB	Fast Event Counters for segments A and B. This is the number of counts per DCE second entering the TDCs from the charge amplifiers. It is minimally affected by dead time as it has a dead time of ~300ns.	variable
DECA DECB	Digitized Event Counter for segments A and B. This is the number of counts per DCE second that make it out of the TDC and are input to the round robin. FEC is normally greater than DEC due to dead time.	variable
SDC1 SDC2	Science Data Counters. This is the number of events clocked out of the round robin, and is equal to the sum of DECA and DECB. The two SDCs are a redundant count of the same thing, and *do not* correspond to the two segments. They can be different by a count or two due to timing and display.	variable
CNTA CNTB	Count rate protection limit. It is a sliding boxcar sum of 10 cycles. If the FECA or FECB rates exceed their respective limits the flight software will turn the HV to HVLow.	20,000
INTA INTB	Interval in seconds over which you integrate for the count rate protection. Nominal value 10 seconds.	= 0 disabled = 10, nominal

4.2.6 Voltages

Voltages at various locations on the detector. The range of the voltage digitized at the ADC is from 0-5V. **Since these are regulated voltages, they should normally not change. If they do it is indicative of a serious problem.**

ID	Description	Value
PMON	Power monitor, total voltage.	52 W
P5TA	TDC A +5V	5.0 V
P5TB	TDC B +5V	4.9 V
P15TA	TDC A +15V	15.0 V
P15TB	TDC B +15V	14.9 V
M5TA	TDC A -5V	-5.3 V
M5TB	TDC B -5V	-5.3 V
M15TA	TDC A -15V	-15.2 V
M15TB	TDC B -15V	-15.2 V
P5DA	DCE A +5V	5.0 V
P5DB	DCE B +5V	5.0 V
P5DC	DCE C +5V	5.0 V
P15D	DCE +15V	15.2 V
M15D	DCE -15V	-15.2 V

4.2.7 Temperatures

Temperatures for various components of the detector for each segment. A lower value corresponds to a higher temperature. 129.4˚C is not a real value; it indicates that this temperature monitor is not enabled.

ID	Description	Value	
ACT	Door actuator	24.2 ˚C	
IP	Ion pumps	24.5 ˚C	
HVFM	High voltage filter module	24.9 ˚C	
LVPC	Low voltage power converter	28.9 ˚C	
HVPS	High voltage power supply	28.9 ˚C	
DCE	Detector control electronics	28.6 ˚C	
		A	B
TDC	Time to digital converter	31.3 ˚C	32.4 ˚C
DVA	Detector vacuum assembly	24.5 ˚C	24.5 ˚C
AMP	Amplifiers	26.0 ˚C	25.7 ˚C

4.2.8 Door State

These values are only valid if AXPWR is on (see Door Motor and Actuator box below).

Name	Description	Values
CL	Closed. Indicates whether door is closed or not.	0 = not closed 1 = closed
POS	Door position. This value has an 8-bit range.	~200 = open ~15 = closed (values vary slightly w/ temperature)
OP	Open. Indicates whether door is open or not.	0 = not open 1 = open
LA	Latch (clam shell). In normal operation LA is 0.	0 = latched 1 = unlatched
TIMER	Timer that counts down from value of 230 seconds. The door takes 3:10 (190sec) to close and a pad of 30 seconds is added to this. This value has an 8-bit range.	

4.2.9 Door Motor and Actuator

When the door is operated, the values in this box are populated in the order they occur (i.e., starting at the top and moving downward).

Name	Description	Values
AXPWR	Auxiliary power	0 = off 1 = on
AXI	Auxiliary current	10 (raw units)
ILIM	Current limit	75 (raw units) operationally dependent
MENA	Motor enabled	0 = motor disabled 1 = motor enabled
MDIR	Motor direction	0 = safe 1 = open 2 = close
MPWR	Motor power	0 = off 1 = on
ACTEN	Actuator enabled	0 = disabled 1 = enabled
ACT1, ACT2	Actuators 1 and 2 correspond to the	= 1 if powered

	redundant windings for the actuator. There are not two actuators.	= 0 if not
LSOVD	Limit switch override. If this is set to 1 the door will ignore the limit switch values.	
AXAN	Auxiliary analog	
MTRAN	Motor analog	
ACTAN	Actuator analog	
PLUG	Safety plug status. It has to be OUT for the door to operate.	1 = good to go, plug OUT 0 = not good to go, safety plug is IN

4.2.10 Digitizer Settings

The digitizer settings refer parameters which control how the time-to-digital converters analyze a photon event. Once set, the should never change except by a couple of counts.

Name	Description	Values
LQT	Lower charge threshold (does not affect FEC, only DEC)	128 (raw units)
UQT	Upper charge threshold	
REF	Reference value	
STIM	State of STIMs	0 = off 1 = 2 cts/sec 2 = 30 cts/sec 3 = 2000 cts/sec
SHF, STR	Shift offset and stretch (scale) of image	
TT	timing threshold (can change the FECs)	
BW, EW	begin walk and end walk (they affect the detector performance)	

4.2.11 HV Presets

Name	Description	Values
VILIM	Current monitor limit. If you are at or above this limit for longer than the persistence time (20msec) the HV shuts down. It is sampled once every 4msec. **THIS IS ONE OF THE KEY SAFETY LIMITS IN THE SYSTEM.**	
VLO	HVlow state voltage. (reported as positive even though they are negative voltages)	0 = 2500V
VNOM	HVNom state voltage.	

VMAX	Maximum allowed value for high voltage. You cannot command it above this value, the software does not allow it - you get an error.	
VTGT	Target voltage when ramping. You cannot command VTGT above VMAX, and you cannot command VMAX below VTGT.	
RAMPT	Ramp time between steps in tenths of second.	0 = delta function 10 = nominal
PLUG	Indicates absense of SAFE plug, i.e. enabled stated.	1 = good to go 0 = not good to go (external plug present)

4.2.12 HV Status

Name	Description	Values
STATE	High voltage state.	0 –7 (see Chstate on page 24 for details)
VENA	Voltage enabled.	0 = no 1 = yes
VQPWR	QE grid voltage	0 = off 1 = on
VPWR	HV power	0 = off 1 = on
FAN	Rear field HV analog.	~11 nominal
IMON	Current to the MCP in microamps. It is checked every 4ms by DCE FSW.	
VSET	Indicates what the HVPS control DAC voltage is set at. Value range 0-255; 15.69V/step. There is an offset of (-)2500 V.	1 = -2500V
VMON	Voltage from the talk-back monitor at the plates. 25V/step, 100 at turn on.	
QAN	Analog talk-back for the QE grids.	Nominal ~ 13
RMP	Ramping or not.	0 = not ramping 1 = ramping

4.2.13 HK Pulse Heights (A,B)

The accumulated pulse height distribution for segment A,B that is continually updated while the detector is on.

Max: first value is the x-axis (channel) location of maximum of the pulseheight; second value is the y-axis (pulse height) value of the maximum.

Cursor: Click on the plot to get a reading of the value of the counts and channel at the location of the cursor.

4.3 COMMAND INTERFACE

The user operates the detector through a series of procedures, functions and commands. All of these are typed from a UNIX prompt on the SUN workstation described in section 3. Some of these functions (not all of them), if issued with no or invalid parameters, will display a message in the terminal window describing its usage and parameters. The command has been completed (successfully or not) when the UNIX prompt reappears in the terminal window.

5. STANDARD OPERATIONS

The FUV detector produces science data in the form of event dispersion (IMAGE-X) and cross-dispersion (IMAGE-Y) positions and pulse height. Events will be detected and processed when the electronics are powered and the high voltage is on and set high enough that the event pulse height exceeds the charge threshold. The operational configuration of the FUV detector is to then send these events in digital form (14 bit IMAGE-X, 10 bit IMAGE-Y, 7 bits of PH, 1 bit segment ID) to the detector EGSE. Once on at nominal HV, no commands to the FUV detector are required to start or to stop data flow.

The following seven FUV detector states are used in controlling the detector (see Figure 5.1-1):

- FUV Hold (FUVHold): the FUV subsystem is off.
- FUV Boot (FUVBoot): the state after a power-on (or other) reset. The Boot state loads a code image whose functionality is restricted to allowing an upload of the software image from the MEB to RAM.
- FUV Operate (FUVOper): the FSW code image is loaded and running, and all system presets are loaded.
- FUV HV LOW (FUVHVLow): the FUV detector is operating with HV to both segments at a low value.

- FUV HV Nominal (FUVHVNom): the FUV detector is operating with HV to both segments on at a nominal detector setting.
- FUV HV Segment A (FUVHVsgA) : the nominal HV is on for segment A only.
- FUV HV Segment B (FUVHVsgB): the nominal HV is on for segment B only.

5.1 STARTING DETECTOR OPERATIONS

- On the cos sparc station that runs the detector the operator needs to login using the carefully distributed username and password.
- For every test, start in a new directory with new Config, Log,, etc., files. The Autolog file is automatically started by the GSE software.
- *Set up a working directory*:

  The convention used in creating a working directory is described in UCB-COS-SPC-1130A.
- *Set up Config file* by copying the Config file from the previous directory and edit appropriately.

  Captures all the hardware setup information, tracking #s on hardware, bias angles on MCPs, etc.
- *Set up Log file* (manually enter information). Copy the header info from the last Log file and edit those items which describe the test, operator, date, etc.
- Stim fits files are also automatically created at ***Pon***. ***Pon*** and ***Poff*** call ***Fgstim***, which creates these files.
- If you type, e.g., Fr ctl-d you get a list of all the Fr commands.

5.2 FUV DETECTOR COMMANDING

The FUV detector system can be commanded by the user from the UNIX prompt in the command window. The detector is operated through a series of commands, functions and procedures. Commands are single commands to the DCE. Functions and procedures issue a series of commands. These are written as either shell or perl scripts. A procedure or function will call a number of commands to bring the system to a desired state or perform some operation. These command scripts call programs which send the proper character strings to the communication port on which the detector system receives information/commands. The operator should be able to use the system in a normal fashion using only procedures and functions. Under normal conditions, an operator will never need to issue commands, only procedures and functions. Nonetheless, commands are covered here for completeness. Particular attention should be paid to the ***Csafe*** command, which should be used in case of an emergency to place the detector in a safe configuration (it immediately removes HV and door power).

5.2.1 Commands

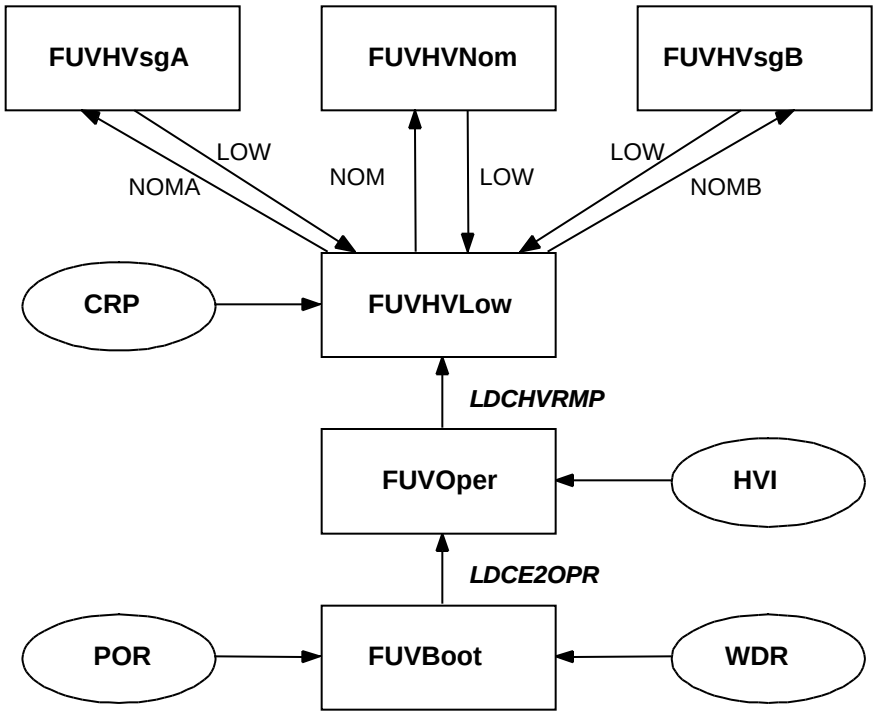


Figure 5.1-1: States of the FUV detector.

The commands available from the UNIX prompt are meant to perform the similar operations as the commands described in the Appendix B of the DM-05 document "COS CS FSW to DCE FSW COMMAND Descriptions". All commands start with the capital letter "C". In general, the second letter indicates if the command operates on the DCE (d), the Digitizer (g), the High Voltage (h) or the Door (r). Below is a short description of the commands available.

NAME	Description	Usage	Parameters
Cdcopy	Memory-to-memory copy	Cdcopy SAddr DAddr Length Bank	SAddr: Source DCE Memory Address (hex) [0-0xFFFF] DAddr: Destination DCE Memory Address (hex) [0-0xFFFF] Length: DCE Memory Load Length, in bytes (hex) [0-0xFFFF] Bank: Memory Monitor Bank select (Decimal) [0-1]
Cdcrc	Calculate CRC on DCE memory range	Cdcrc Addr Length Bank	Addr: DCE Memory Address (hex) [0-0xFFFF] Length: DCE Memory Load Length, in bytes (hex) [0-0xFFFF] Bank: Memory Monitor Bank select (Decimal) [0-1]
Cddiagc	Clear diagnostic code stack	Cddiagc	None
Cddnlod	Download memory block	Cddnlod Addr Length	Addr: DCE Memory Address (hex) [0-0xFFFF] Length: DCE Memory Load Length, in bytes (hex) [0-0x400]
Cdgoto	Jump to specified address and execute	Cdgoto DAddr	DAddr: Destination DCE Memory Address (hex) [0-0xFFFF]
Cdhkreq	Send full housekeeping frame	Cdhkreq	None
Cdjmpcs	Jump to upper/lower code segment	Cdjmpcs	None
Cdmaddr	Sets MEB Monitor Address	Cdmaddr Index Addr Byte	Index: Memory Monitor Index (Decimal) [0-7] Addr: DCE Memory Address (hex) (Hex) [0-0xFFFF] Byte: Analog setting (Decimal) [0-2]
Cdnoop	No Operation	Cdnoop	None
Cdrsta	Actel Reset – Toggles port # (P1.7) on the 80501	Cdrsta	None
Cdrstp	Power On Reset	Cdrstp	None
Cdrstw	Watchdog Reset	Cdrstw	None
Cduplod	Memory upload	Cduplod Daddr Length CRC	DAddr: Destination DCE Memory Address (hex) [0-0xFFFF] Length: DCE Memory Load Length, in bytes (hex) [0-0x400] CRC: CRC Value (hex) (Hex) [0-0xFFFF]
Cdwdog	Watchdog disable/enable	Cdwdog Set	Set: Disable=0, Enable=1 (Binary)

Cgbwk	TDC Begin Walk Adjust	Cgbwk Byte Seg Axis	Byte: Analog setting (Decimal) [0-255] Seg: Detector Segment. A=0, B=1 (Binary) [0,1] Axis: Image Axis. X=0, Y=1 (Binary) [0,1]
Cgewk	TDC End Walk Adjust	Cgewk Byte Seg Axis	Byte: Analog setting (Decimal) [0-255] Seg: Detector Segment. A=0, B=1 (Binary) [0,1] Axis: Image Axis. X=0, Y=1 (Binary) [0,1]
Cdrsts	Speical Reset	Cdrsts	None
Cglqt	TDC A Lower Charge Threshold	Cglqt Byte Seg	Byte: Analog setting (Decimal) [0-255] Seg: Detector Segment. A=0, B=1 (Binary) [0,1]
Cgshft	Segment Image Shift	Cgshft Byte Seg Axis	Byte: Analog setting (Decimal) [0-255] Seg: Detector Segment. A=0, B=1 (Binary) [0,1] Axis: Image Axis. X=0, Y=1 (Binary) [0,1]
Cgstim	Stim control, on/off, rate	Cgstim StimMode Seg	StimMode: 0=OFF, 1=2cps, 2=30cps, 3=2000cps (Decimal) Seg: Detector Segment. A=0, B=1 (Binary) [0,1]
Cgstr	Segment Image Stretch	Cgstr Byte Seg Axis	Byte: Analog setting (Decimal) [0-255] Seg: Detector Segment. A=0, B=1 (Binary) [0,1] Axis: Image Axis. X=0, Y=1 (Binary) [0,1]
Cgtt	TDC Timing Threshold	Cgtt Byte Seg Axis	Byte: Analog setting (Decimal) [0-255] Seg: Detector Segment. A=0, B=1 (Binary) [0,1] Axis: Image Axis. X=0, Y=1 (Binary) [0,1]
Cguqt	TDC Upper Charge Threshold	Cguqt Byte Seg	Byte: Analog setting (Decimal) [0-255] Seg: Detector Segment. A=0, B=1 (Binary) [0,1]
Chqpwr	QDE Grid HV On/Off	Chqpwr Set	Set: Disable=0, Enable=1 (Binary) [0,1]
Chrampt	HV Ramp time constant	Chrampt Byte	Byte: Analog setting (Decimal) [0-255]
Chstate	Set HV state	Chstate State	State: HVState [0-4] 1=NomA: A Nom, B Low 2=Nom B: A Low, B Nom, 3=NomAB: A Nom, B Nom 4=Low: A Low, B Low
Chvena	HV power supply enable/disable	Chvena Set	Set: Disable=0, Enable=1 (Binary) [0,1]
Chvilim	HV current limit setting	Chvilim Byte	Byte: Analog setting (Decimal) [0-255]
Chvlow	HV level for HVLOW state	Chvlow Byte Seg	Byte: Analog setting (Decimal) [0-255] Seg: Detector Segment. A=0, B=1 (Binary) [0,1]
Chvmax	Maximum level for HV	Chvmax Byte Seg	Byte: Analog setting (Decimal) [0-255] Seg: Detector Segment. A=0, B=1 (Binary) [0,1]
Chvnom	HV level for HVNOM state	Chvnom Byte Seg	Byte: Analog setting (Decimal) [0-255] Seg: Detector Segment. A=0, B=1 (Binary) [0,1]
Chvpwr	HV Power Supply On/Off	Chvpwr Set	Set: Disable=0, Enable=1 (Binary) [0,1]
Chvset	MCP HV level Setting	Chvset Byte Seg	Byte: Analog setting (Decimal) [0-255] Seg: Detector Segment. A=0, B=1 (Binary) [0,1]
Cpcrp	CRP Algorithm Parameters	Cpcrp Int Seg Cnt	Int: CRP Smoothing Interval, (Decimal) [0-255] Seg: Detector Segment. A=0, B=1 (Binary) [0,1] Cnt: CRP Rate Threshold (Decimal) [0-65535]

Cract1	Actuator1 On/Off	Cract1 Set	Set: Disable=0, Enable=1 (Binary) [0,1]
Cract2	Actuator2 On/Off	Cract2 Set	Set: Disable=0, Enable=1 (Binary) [0,1]
Cracten	Actuator Control Enable/Disable	Cracten Set	Set: Disable=0, Enable=1 (Binary) [0,1] 0 = Abort, 1 = Relatch
Cractrs	Actuator Reset	Cractrs Set	Binary [0,1]
Craxpwr	Aux Power Supply On/Off	Craxpwr Set	Set: Disable=0, Enable=1 (Binary) [0,1]
Crilim	Door Motor / Actuator / HVPS Current Limit setting	Crilim Byte	Byte: Analog setting (Decimal) [0-255]
Crlsovd	Door limit switch override	Crlsovd Set	Set: Disable=0, Enable=1 (Binary) [0,1]
Crmdir	Select the door direction	Crmdir Direction	Direction: 0=Safe, 1=Open, 2=Close (Decimal) [0,1,2]
Crmena	Door Motor Enable	Crmena Set	Set: Disable=0, Enable=1 (Binary) [0,1]
Crmpwr	Power Door Motor On/Off	Crmpwr Set	Set: Off =0, On =1 (Binary) [0,1]
Csafe	Safe FUV Detector	Csafe	None

5.2.2 Functions

Below is a list of available functions as of this writing. All of these are meant to perform a specific task or put the system in a specific state. Some of these functions have prerequisites on the system before they can be issued.

Name	**Description**	**Prerequesites**	**Parameters**	**Commands Called**
Fbkg	Collects a background image of 2500 events as defined in parameter file bkg.pf used by sci2xyp. Writes 2 FITS files (1 for each seg.) named cosxyp_dt_tm_seg.fits where dt is the date, tm is the time and seg is the segment A or B example: cosxyp001122-121943_A was taken on Nov 22, 2000 at 12:19:43 on segment A	Power on digitizers set HV on	None	cosnoopy Cgstim 1 0 Cgstim 1 1 sci2xyp –p bkg.pf lg
Fcreport	Reports status of counters at the terminal and in the Autolog file	Power on	None	hkprint_dec cnt_deca hkprint_dec cnt_decb hkprint_dec cnt_feca hkprint_dec cnt_fecb hkprint_dec cnt_sdc1 hkprint_dec cnt_sdc2 hkprint_dec cnt_time

				hkprint_dec cnt_pkt lg
Fdalive	Verifies COS DCE and EGSE are alive. Prints a message on the screen and in the Autolog file with status of DCE (ALIVE or not ok)	Power on	None	cosnoopy hkprint cnt_time sleep 1 hkprint cnt_time Cdnoop lg
Fdeepflat	Collects a deep flat image for 1 hour exposure with stims on at 2cps as described in parameter file deepflat.pf used by sci2img. Writes 4 FITS files: count_image and ph_image for each segment	Power on, digitizers set HV on	None	cosnoopy Cgstim 1 0 Cgstim 1 1 lg sci2img –p deepflat.pf
Fdhkver	Verifies operation of housekeeping. Prints a message on the screen and in the Autolog file with the result (OK or not OK)	Power on	None	cosnoopy hkprint dig_uqta Cguqt 0 0 sleep 1 hkprint dig_uqta Cguqt 255 0 sleep 1 hkprint dig_uqta lg
Fdumpbuffers	Dumps HVI and AUXI sample buffer and Histogram areas in current directory as: auxistr.buf, auxistr.hst hvistr_a.buf, hvistr_a.hst hvistr_a.buf, hvistr_b.hst *note: “str” is an optional input to the command	OPERATE Mode v1028 or higher	str	cosnoopy sendcmd aeae e000 400 hkprint 0x1040-0x143f sendcmd aeae e400 200 hkprint 0x1040-0x143f sendcmd aeae e600 400 hkprint 0x1040-0x143f sendcmd aeae ea00 200 hkprint 0x1040-0x143f sendcmd aeae ec00 400 hkprint 0x1040-0x143f sendcmd aeae f000 200 hkprint 0x1040-0x143f
Fflat	Collects a Flat Image of 10 minutes exposure time and stims at 30cps. Writes 4 FITS files: flat_dt_tm_seg.fits flat.ph_dt_tm_seg.fits	Power On Digitizers set HV on	None	cosnoopy Cgstim 2 0 Cgstim 2 1 sci2img –p flat.pf lg
Fgainvolt	Collects 100,000 events with stims at 30cps and writes 2 FITS files: gv_dt_tm_seg.fits	Power On Digitizers set HV on	None	cosnoopy Cgstim 2 0 Cgstim 2 1 sci2xyp –p gainvolt.pf lg
Fgreport	Reports on digitizers values on the terminal and in the Autolog file	Power on	None	hkprint_dec dig_shfax hkprint_dec dig_shfay hkprint_dec dig_shfbx

				hkprint_dec dig_shfby hkprint_dec dig_strax hkprint_dec dig_stray hkprint_dec dig_strbx hkprint_dec dig_strby hkprint_dec dig_uqta hkprint_dec dig_uqtb hkprint_dec dig_lqta hkprint_dec dig_lqtb hkprint_dec dig_ttax hkprint_dec dig_ttay hkprint_dec dig_ttbx hkprint_dec dig_ttby hkprint_dec dig_bwkax hkprint_dec dig_bwkay hkprint_dec dig_bwkbx hkprint_dec dig_bwkby hkprint_dec dig_ewkax hkprint_dec dig_ewkay hkprint_dec dig_ewkbx hkprint_dec dig_ewkby
Fgset	Downloads digitizers settings for segment A and B to DCE	Power On	None	cosnoopy Cglqt 0B 0 Cguqt FF 0 Cgtt D0 0 0 Cgbwk 60 0 0 Cgewk 64 0 0 Cgstr 20 0 0 Cgshft 88 0 0 Cgtt D0 0 1 Cgbwk 60 0 1 Cgewk 60 0 1 Cgstr 80 0 1 Cgshft 70 0 1 Cglqt 0B 1 Cguqt FF 1 Cgtt D0 1 0 Cgbwk 64 1 0 Cgewk 64 1 0 Cgstr 44 1 0 Cgshft AE 1 0 Cgtt D0 1 1 Cgbwk 60 1 1 Cgewk 60 1 1 Cgstr 78 1 1 Cgshft b4 1 1
Fgstim	Collects image of stims with 10000 counts for segments A and B. Writes 2 FITS files, one for each	Power on digitizers set	None	cosnoopy Cgstim 3 0 Cgstim 3 1

	segment with time tag data as: stim_dt_tm_seg.fits where dt is the date and tm is the time			sci2xyp –p stim.pf lg IDL Fgstimanal
Fhlow	Turns HV to "LOW" setting. The housekeeping monitor window will show the voltage VSET increase to the predefined HVLO value.	Fhset	None	cosnoopy Chvena 1 Chpwr 1 Chqpwr 1 Chstate 4 lg
Fhnom	Turns HV to "NOMINAL" setting. The monitor window will show the voltage VSET increase to the predefined HVNOM value.	Fhlow	None	cosnoopy Cgstim 0 0 Cgstim 0 1 Chstate 3 lg
Fhoff	Turns off HV		None	cosnoopy Chqpwr 0 Chvpwr 0 Chvena 0 lg
Fhpoff	Turns OFF Power Supply Unit via the GPIB interface		None	
Fhpon	Turns ON Power Supply Unit via the GPIB interface		Voltage: between 18-32v Defaults to 28v if absent	
Fhreport	Reports status of HV to the screen and the Autolog file	Power ON	None	hkprint_dec hv_fan hkprint_dec hv_imona hkprint_dec hv_imonb hkprint_dec hv_vmona hkprint_dec hv_vmonb hkprint_dec hv_qana hkprint_dec hv_qanb hkprint_dec hv_vseta hkprint_dec hv_vsetb lg
Fhset	Sets HV parameters	Power on digitizers set. Count rate protection set	None	cosnoopy Chilim 128 Chrampt 10 Chvmax 161 0 Chvmax 158 1 Chvnom 161 0 Chvnom 158 1 Chvlow 100 0 Chvlow 100 1 lg
Fractfire	Fires Door Actuator 1 or 2	Power ON FUV pressure	None	cosnoopy hklog –p hklogrfire.pf

		must be the same as the VHA pressure		raxpwr 1 rilim 0 racten 1 ract1 1 OR ract2 1 lg
Fractrst	Resets Door after Actuator Firing	Power on door in unlatched state	None	cosnoopy hklog –p hklogrrst.pf Craxpwr 1 Crmena 1 Crilim 0 Cractrs 1 Crilim 90 lg
Frclose	Closes door	Power on	None	cosnoopy hklog –p hklogrclose.pf Craxpwr 1 Crmena 1 Crilim 0 Crmdir 2 Crmpwr 1 Crilim 75 lg
Fropen	Opens door	Power on	None	cosnoopy hklog –p hklogropen.pf Craxpwr 1 Crmena 1 Crilim 0 Crmdir 1 Crmpwr 1 Crilim 75 lg
Frreport	Report status of AUX system on the screen and in the Autolog file	Power on	None	hkprint_dec door_actan hkprint_dec door_mtran hkprint_dec door_axi hkprint_dec door_axan hkprint_dec door_op hkprint_dec door_cl hkprint_dec door_la hkprint_dec door_axpwr hkprint_dec door_mpwr hkprint_dec door_pos lg
Frstop	Stops door movement	DCE OPERATE code v1028 or higher	None	cosnoopy Csafe lg
Ftreport	Reports temperature values on the screen and in the Autolog file	Power on	None	hkprint_dec temp_dvaa hkprint_dec temp_dvab hkprint_dec temp_ampa hkprint_dec temp_ampb hkprint_dec temp_tdca

				hkprint_dec temp_tdcb hkprint_dec temp_act hkprint_dec temp_hvfm hkprint_dec temp_hvps hkprint_dec temp_ip hkprint_dec temp_lvpc hkprint_dec temp_dce lg
Fvreport	Reports voltage on the screen and in the Autolog file	Power on	None	hkprint_dec volt_p5da hkprint_dec volt_p5db hkprint_dec volt_p5dc hkprint_dec volt_p15ta hkprint_dec volt_p15tb hkprint_dec volt_m15ta hkprint_dec volt_m15tb hkprint_dec volt_p5ta hkprint_dec volt_p5tb hkprint_dec volt_m5ta hkprint_dec volt_m5tb hkprint_dec volt_p15d hkprint_dec volt_m15d hkprint_dec volt_pmon lg

5.2.3 Procedures

Below is a list of available procedures as of this writing. All of these are meant to perform a specific task or put the system in a specific state.

Name	Description	Prerequesites	Parameters	Commands Called
PCEset	Prepares system for Emissions testing	Power on	None	Cgstim 2 1 Cgstim 2 0 Fhon Craxpwr 1 lg
PCSset	Prepares system for susceptibility testing	Power on	None	cosload Fgset Fgstim Fdhkver Craxpwr 1 lg
Poff	Turns off system	None	None	Fgstim Csafe coskill Fhpoff lg

Pon	Turns on system in readiness for experiments	None	None	Fhpon cosegse cosload Fgset Fhset Fgstim lg
Ptag	Record data forever until interrupted with CTRL-C, then exit cleanly	Power on	None	sci2xyp –p stimforever.pf hklog –p hklog1s.pf lg
Pvmargin	Performs voltage margin tests	Power on	None	Fhpoff Fhpon 21 Fhpon 18 Fhpon 21 Pshortfunc Fhpoff Fhpon 29 Fhpon 32 Fhpon 29 Pshortfunc lg

5.2.4 Other Routines

Below is a list of other programs the system uses. These routines are called by either commands, functions or procedures. A short description and expected parameters is given here.

Name	**Description**	**Prereqesites**	**Parameters**	**Commands Called**
cosegse	Routine called by Pon to initialize the system	Power on	None	bitload ipcrm cos_shminit costag cmd_server ipcs uptime cosnoopy hklog rtmon
coskill	Kills a number of running processes started by cosegse	None	None	ipcrm rtmon cmd_server cmd_client

				noopy cosnoopy hklog
cosload	Performs POR to put system in BOOT, Loads OPERATE code, Jumps to OPERATE, Enables Watchdog, Sets ups OPERATE memory monitors	cosegse	None	cosnoopy Cdrstp Cdnoop ~/DCEv/DCEOPER_v1039.sh sendcmd Cdjmpcs Cdwdog Cdmaddr
cosnoopy	Calls dnoop every second indefinitely	cosegse	None	dnoop
cospath	Sets UNIX path for COS cmds	Environment variable cossrc defined	None	Cossrc=/disks/cos/users/eagcos/egse/beta/src
fixidl	Sets IDL environment variables	None	None	
hklog	FITS logging of housekeeping monitors		-p paramfile -f filename	
Chknew	Starts a new housekeeping log	None	None	hklog
lg	Copies information to the log file ‘Autolog’	None	A string	
sci2img	Acquire FITS image for counts and gain maps as defined in the specified parameter file.	None	-p Paramfile -c count_file -g gainfile	
sci2xyp	Creates FITS logging of photons in binary table format as defined in the specified parameter file.	None	-p Paramfile -f Filename	

sendcmd	Takes the OPCODE and parameters and forms then sends the command	None	OPCODE Par0 Par1 Par2 Par3 Par4	

6. ANOMOLOUS & EMERGENCY CONDITIONS

6.1 DIAGNOSTICS

The DCE FSW provides a variety of internal limits monitoring and self integrity checks. When it detectors an anamolous condition, it reports a diagnostic message in housekeeping telemetry – in addition issuing an HST Error message.

For Detector Thermal-Vacuum testing at CASA-ARL, Detector Operators should concentrate their attention on the Diagnostic Stack Errors – as this push-down stack provides a history of the last 32 diagnostics issued by the DCE FSW.

In general, a diagnostic is an indication of a problem – which should result in action being taken by the Detector Operator. The following table outlines the various diagnostics in both BOOT and OPERATE modes – and the Action that should be taken by the Detector Operator.

Diagnostic	BOOT	OPERATE	Description	Type of Action	Detector Operator Action
01	x	x	UPLOAD length out of range (<1, >1024)	••	Stop script execution. Contact Detector TC.
02	x	x	UPLOAD bad CRC	••	Stop script execution. Contact Detector TC.
03	x	x	DOWNLOAD length out of range (<1, >1024)	••	Stop script execution. Contact Detector TC.
04	x	x	Command MS-bit must be '1'	••	Stop script execution. Contact Detector TC.
05	x	x	Command opcode must have twin	••	Stop script execution. Contact Detector TC.
06	x	x	Command parameter bad complement	••	Stop script execution. Contact Detector TC.

08		x	HV not enabled. A LFHVENA command is required.	••	Stop script execution. Contact Detector TC.
0B		x	Motor not enabled. A LFRMENA command is required.	••	Stop script execution. Contact Detector TC.
10		x	Door actuators not enabled. A LFRACTEN command is required.	••	Stop script execution. Contact Detector TC.
11	x	x	Illegal command	••	Stop script execution. Contact Detector TC.
13	x	x	Command did not complete execution	••	Stop script execution. Contact Detector TC.
15		x	Actuator already latched, LFRACTRS command ignored.	••	Stop script execution. Contact Detector TC.
16		x	AUX Current exceeded LFRILIM during HV Operations.	•	Note Time of event in Detector Operator's log.
17	x	x	8051 Stack Growth error	•••••	Reset DCE. Contact Detector TC.
1B	x		Power-On Reset	• / ••	On Power-ON "OK" - Otherwise, stop script execution. Contact Detector TC.
1C	x		Watchdog Reset	••	Stop script execution. Contact Detector TC.
1F	x	x	Commanded reset failure	••	Stop script execution. Contact Detector TC.
22		x	CRP shutdown due to excessive counts in the Fast Event counter (FEC).	••	Stop script execution. Contact Detector TC.
26		x	AUX current exceeded door current limit. Door motor and actuators safed.	••	Stop script execution. Contact Detector TC.
27		x	HV-A current exceeded limit ONE time	•	Note Time of event in Detector Operator's log.
28		x	HV-B current	•	Note Time of event in Detector

			exceeded limit ONE time		Operator's log.
2A		x	HV-A current exceeded limit past persistence	••	Stop script execution. Execute Fdumpbuffers. Contact Detector TC.
2B		x	HV-B current exceeded limit past persistence	••	Stop script execution. Execute Fdumpbuffers. Contact Detector TC.
2E		x	Aux current exceeded limit past persistence	••	Stop script execution. Execute Fdumpbuffers. Contact Detector TC.
2F	x		OPERATE mode command received while in BOOT mode	••	Stop script execution. Contact Detector TC.
31	x	x	Call to unused Interrupt Service Routine (ISR)	•••••	Reset DCE. Contact Detector TC.
32	x	x	Background CRC error	•••••	Reset DCE. Contact Detector TC.
33		x	Attempt to set Vtarget > Vmax on Seg A	••	Stop script execution. Contact Detector TC.
34		x	Attempt to set Vmax < Vtarget on Seg A	••	Stop script execution. Contact Detector TC.
35		x	Attempt to set Vtarget > Vmax on Seg B	••	Stop script execution. Contact Detector TC.
36		x	Attempt to set Vmax < Vtarget on Seg B	••	Stop script execution. Contact Detector TC.

•	Detector is fine. Note Time in log for information purposes only.
••	Detector FSW is protecting it's HW. Stop script ASAP to isolate problem, and to avoid further script complications.
•••••	Detector FSW is compromised. Reset Detector ASAP to insure HW Safety is maintained.

6.2 TELEMETRY OUT-OF-LIMITS EVENTS

Aside from DCE FSW Detector Health and Safety Monitoring Tasks discussed elsewhere in this document (i.e., Current Limit Protection Task, Count Rate Protection Task, and Door Protection Task) – the DCE FSW does not monitor it's own analog telemetry values for out-of-limits behavior. The HST design approach for this detector was, instead, to put this kind of monitoring within the CS FSW. Since the EGSE for the FUV Detector does not perform autonomous limit checking, like the CS FSW – it is the responsibility of the Detector Operator to monitor the FUV Detector Telemetry and take appropriate actions if an out-of-limits event is detected.

The following table summarizes the current 'best-guess' for FUV Detector Limit Values – and the appropriate action a Detector Operator should take if they see the Detector telemetry consecutively out of limits for more than the persistence period of time.

Mnemonic	Units	Description	Nominal	Low Limit	High Limit	Persistance	Detector Operator Action
LFTACT	ºC	**Actuator temp**	OD	-20	45	1 min	Reset DCE. Contact Detector TC.
LFTAMPA	ºC	**Amp A temp**	?	-20	60	1 min	Reset DCE. Contact Detector TC.
LFTAMPB	ºC	**Amp B temp**	?	-20	60	1 min	Reset DCE. Contact Detector TC.
LFTDCE	ºC	**DCE temp**	?	-20	60	1 min	Reset DCE. Contact Detector TC.
LFTDVAA	ºC	**Det Vacuum Assy A Temp**	22	-20	45	1 min	Reset DCE. Contact Detector TC.
LFTDVAB	ºC	**Det Vacuum Assy B Temp**	22	-20	45	1 min	Reset DCE. Contact Detector TC.
LFTHVFM	ºC	**HVFM temp**	?	-20	60	1 min	Reset DCE. Contact Detector TC.
LFTHVPS	ºC	**HVPS temp**	?	-20	60	1 min	Reset DCE. Contact Detector TC.
LFTIP	ºC	**Ion Pump temp**	OD	-20	60	1 min	Reset DCE. Contact Detector TC.
LFTLVPC	ºC	**LVPC temp**	?	-20	60	1 min	Reset DCE.

LFTTDCA	ºC	**TDC A temp**	?	-20	60	1 min	Contact Detector TC. Reset DCE.
LFTTDCB	ºC	**TDC B temp**	?	-20	60	1 min	Contact Detector TC. Reset DCE.
LFVM15D	V	**DCE -15V**	-15.22	-16.74	-13.70	30 sec	Contact Detector TC. Reset DCE.
LFVM15TA	V	**TDC A -15V**	-15.22	-16.75	-13.70	30 sec	Contact Detector TC. Reset DCE.
LFVM15TB	V	**TDC B -15V**	-15.22	-16.75	-13.70	30 sec	Contact Detector TC. Reset DCE.
LFVM5TA	V	**TDC A -5V**	-5.29	-5.82	-4.76	30 sec	Contact Detector TC. Reset DCE.
LFVM5TB	V	**TDC B -5V**	-5.29	-5.82	-4.76	30 sec	Contact Detector TC. Reset DCE.
LFVP15D	V	**DCE +15V**	15.22	13.70	16.74	30 sec	Contact Detector TC. Reset DCE.
LFVP15TA	V	**TDC A +15V**	14.96	13.46	16.45	30 sec	Contact Detector TC. Reset DCE.
LFVP15TB	V	**TDC B +15V**	14.86	13.37	16.34	30 sec	Contact Detector TC. Reset DCE.
LFVP5DA	V	**DCE-A +5V**	5.00	4.50	5.50	30 sec	Contact Detector TC. Reset DCE.
LFVP5DB	V	**DCE-B +5V**	5.00	4.50	5.50	30 sec	Contact Detector TC. Reset DCE.
LFVP5DC	V	**DCE-C +5V**	4.97	4.47	5.47	30 sec	Contact Detector TC. Reset DCE.
LFVP5TA	V	**TDC A +5V**	5.00	4.50	5.50	30 sec	Contact Detector TC. Reset DCE.
LFVP5TB	V	**TDC B +5V**	4.95	4.45	5.44	30 sec	Contact Detector TC. Reset DCE.
LFVPMON	W	**LVPC Power**	52	0	62	5 min	Contact Detector TC. Reset DCE.

Contact
Detector TC.

6.3 FACILITIES FAILURES

The thermal vacuum (T-V) chamber is a sophisticated facility with numerous interlocks and functions to protect itself. These interlocks are NOT integrated with the flight detector and it is the responsibility of the detector operator to safe the flight detector in the event of a facility related failure.

There are two classes of facility related failures, those that relate to the vacuum environment and those that relate to the thermal environment or it's control. The vacuum environment related failures are the most serious and pose an immediate risk to the health and safety of the detector. Those failure relating to the thermal environment can be serious and require action, however, the time scale for action is measured in tens of minutes. As a general note, if the pressure within the tank is less than 1 X 10^{-4} Torr and the detector door is closed turn on the ion pumps.

If the corrective action is taken for ANY reason call the appropriate test conductor immediately.

6.3.1 Vacuum Problems

If the vacuum in the chamber rises above 1X10^{-5} Torr for any reason the high voltage must be turned off immediately. Following turning off the high voltage the door must be closed. The vacuum can rise for a variety of reasons and it is the responsibility of the detector operator to monitor the pressure regularly. If the pressure is below 1 X 10^{-4} Torr turn on the ion pumps. There is no need to turn off the low voltage power to the detector.

If the gatevalve on the cryogenic pump closes immediately turn off the HV and close the door.

6.3.2 Thermal Problems

If the thermal control system controlling the scavenger plate fails the HV and detector door must be turned off and closed respectively. The scavenger plate collects contamination from within the chamber and if the plate warms up under vacuum it can migrate throughout the chamber contaminating everything in the chamber. Turn on the ion pumps.

If the thermal environment for the detector drops below –25 deg. C turn off the HV and close the door, but do not turn the detector off. The warmth of the electronics may help to protect the detector. **If the thermal environment rises above 50 deg. C then turn off HV, close the door, and turn off the detector**, so that the electronics do not over heat. Turn on the ion pumps.

7. DCE FLIGHT SOFTWARE OVERVIEW

7.1 FUNCTIONAL OVERVIEW

The FUV Detector Control Electronics (DCE) is the main control and coordination center for the FUV Detector Subsystem. It provides the FUV detector with the computational, interface, and memory resources necessary for performing FUV detector control operations. The DCE flight software resides in the DCE and provides the control and status capabilities of the FUV detector.

When power is applied to the FUV Detector Subsystem, the DCE FSW begins executing. The FSW is responsible for initializing its own operating environment and putting the FUV Detector hardware in a known configuration. After the FSW has initialized, it is ready to accept commands and provide status information.

The DCE FSW accepts and validates incoming command packets. The DCE FSW supports commands that configure the digitizers, set voltage limits, ramp the high-voltage, move the door mechanism, and generally support FUV detector operations.

The DCE FSW returns housekeeping data. Housekeeping provides insight into the state of the FUV detector. The FSW collects engineering data and formats it for output via the housekeeping interface. Engineering data comes in many forms including temperatures, voltages, currents and other sensor data that are converted to a digital format.

The DCE FSW provides other necessary functions beyond command and status. It performs internal limit checking of critical detector parameters, reports the rate at which science data events are occurring to protect the FUV detector from an overlight condition, and performs various background checks to ensure the integrity of the operating environment.

Though the DCE FSW controls the FUV detector hardware, it does not process the science data generated by the FUV hardware. The FSW sees only counts and not coordinate information for each photon event. In short, science data does not pass through the DCE FSW.

7.2 CONTROL FLOW

The basic design of the software control flow is that of an initialization sequence followed by an infinite processing loop. This control flow originates with a reset event, such as power-on to the DCE. The main software processing loop, called the executive loop, can be interrupted by a hardware signal that directs the 8051 to execute a special sequence of code called an interrupt service routine (ISR). ISRs are designed to execute quickly and terminate, restoring control to the executive loop at the point it was interrupted. Figure 7.1 shows the System Level Control Flow Diagram to graphically demostrate how the DCE FSW functions.

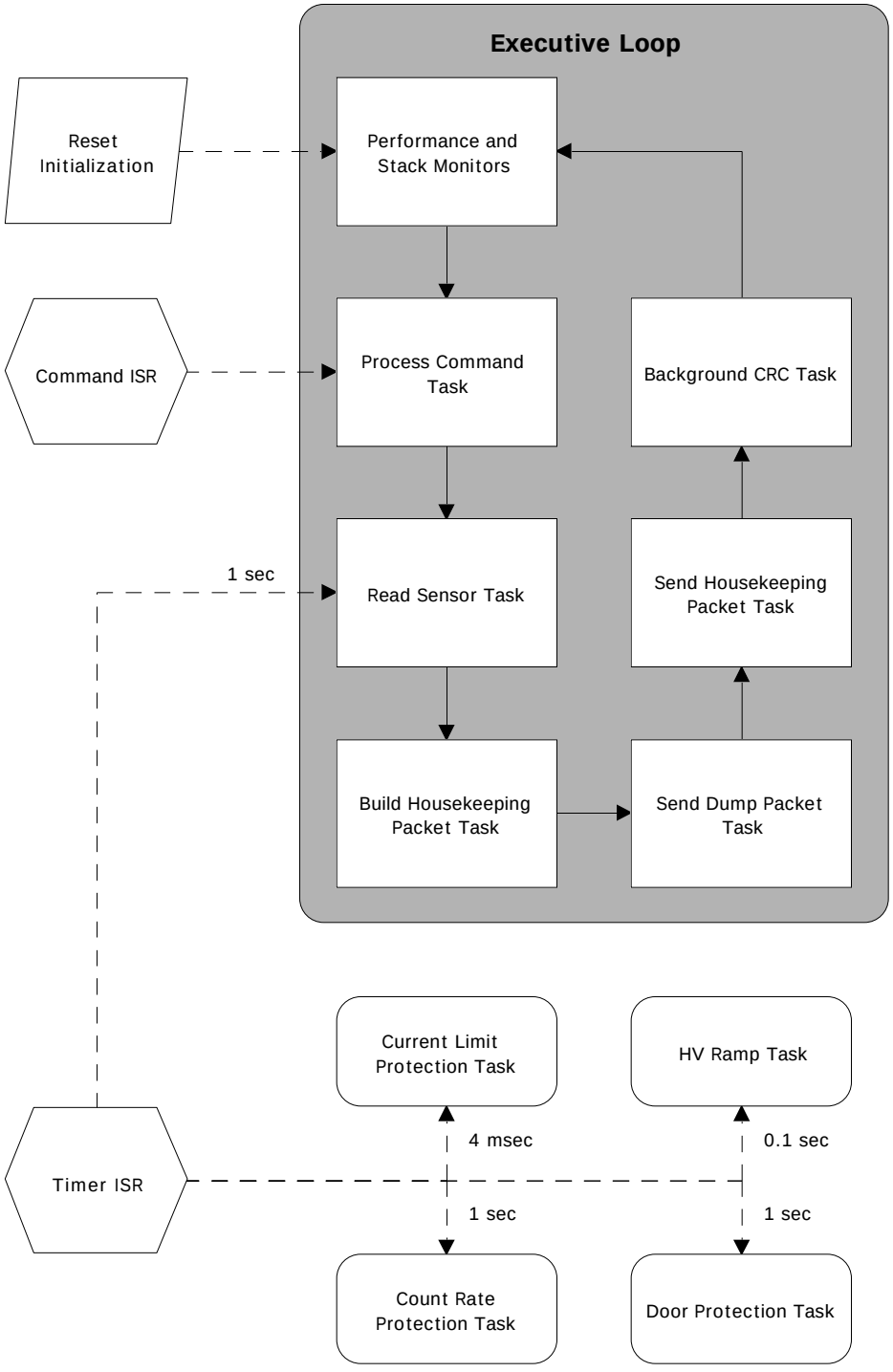


Figure 7-1 is the System Level Control Flow Diagram for the DCE flight software.

7.3 HARDWARE INTERFACES

This section describes the hardware interfaces to the DCE flight software. Hardware interfaces refer to the following:

Internal DCE hardware which the DCE FSW controls and from which it reads status, External hardware from which the DCE FSW receives commands and sends housekeeping data.

Internal hardware refers to the 8051 micro-controller ports and memory mapped I/O addresses used by the DCE FSW to access the FUV hardware. The hardware interfaces are dealt with at a high-level. The intent of this section is to describe the type of hardware control and status that the DCE FSW provides. The low-level commanding of the hardware (i.e. which bits in which register to set or clear) is defined in the DCE Hardware-to-Software Interface section.

This section is broken down into two subsections. The first subsection looks at the interfaces between the DCE FSW and the outside world, and the second subsection examines the interfaces between the DCE FSW and the FUV Detector hardware. Within those two subsections, all of the hardware interfaces are described. Each hardware interface is described in terms of the control provided by the DCE FSW and the status returned by the hardware.

Figure 7.2 (shown below) is the FUV Detector Functional Block Diagram. It provides an overview of the FUV detector hardware. It is included here to provide additional information about the hardware that is controlled by the DCE FSW.

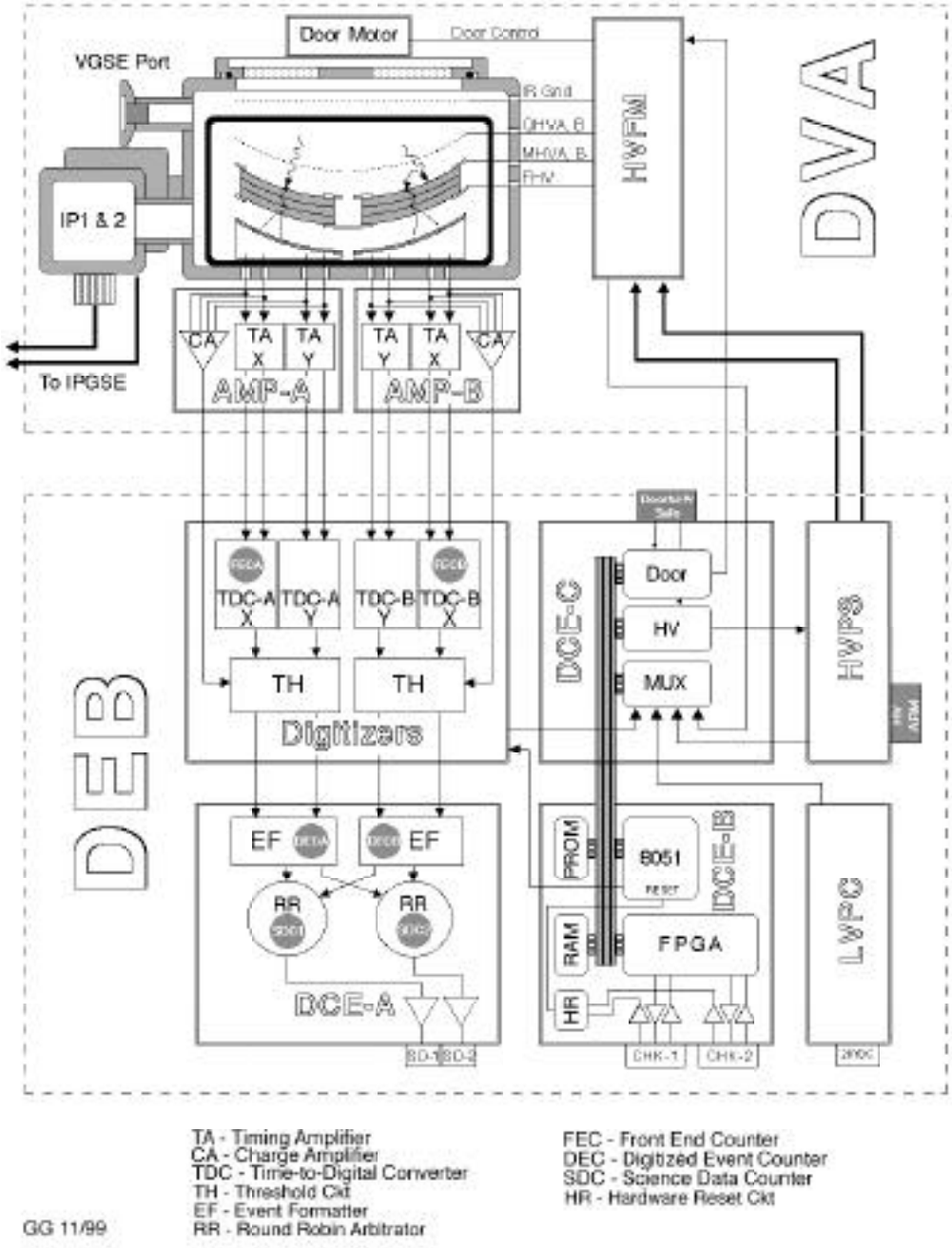


Figure 7-2 FUV Detector Functional Block Diagram

Interfaces Between the DCE FSW and the Outside World

7.3.1.1 Command Registers

All DCE commands are sent via a command link to the DCE. In the DCE, each incoming 32-bit word is transferred into a set of four 8-bit command registers. An 8051 Interrupt is generated when the last of these registers is filled. (See Section 8.2.5). Additionally, a "busy" signal on the command link goes high when a 32-bit word begins to arrive at the DCE. The "busy" signal is an indication to the Outside World that command traffic should pause until the DCE has processed the 32-bit data in the command registers. The Command ISR in the DCE FSW reads the command registers, and then returns control flow to the executive loop. The act of reading the last of the 8-bit registers by the DCE FSW clears the command-line "busy" signal, notifying the Outside World that the next 32-bit value can be placed into the command registers.

The DCE has two redundant command links, A and B, which are both always active. Each link has it's own set of four 8-bit registers. Either link may be used to command the DCE at any time. The DCE FSW receives a primary or secondary command link interrupt – depending upon which of the two command links has received the 32-bit data – and resulting ISR calls a procedure to read the 32-bit command word from the appropriate registers.

7.3.1.2 Housekeeping Registers

The housekeeping interface between the DCE and the outside world is similar to the commanding interface. The DCE uses four 8-bit registers that serially shift out data across the command link. The DCE FSW writes each 32-bit housekeeping word to the housekeeping registers and the DCE hardware takes care of shifting out the data across the command link. Housekeeping data is always written out across both command links.

7.3.2 Interfaces Between the DCE FSW and the FUV Detector Hardware

7.3.2.1 Control Registers

The DCE FSW controls the high-voltage power supply (HVPS) and the door mechanism by setting and clearing bits in one of two control registers. The control bits that can cause severe degradation to the FUV detector if used incorrectly are allocated to a protected control register that has been equipped with a lock bit. The use of the lock bit is described in Section 8.3.1. The remaining control bits that cannot directly cause damage to the FUV detector have been allocated to an unprotected control register.

7.3.2.1.1 Protected Control Register

The protected control register contains control bits that can immediately cause damage to the FUV detector if used incorrectly. The control bits allocated to this register are as follows:

Door Override – Overrides the Door End Switch indicators – allowing the motor to drive beyond the normal door open/close positions. (Note: The Override is needed to 'relatch' the door when it has been opened via the Actuator.)
Actuator enable - Enables/disables actuator support circuitry which allows the actuators to be powered.
Actuator power – Powers the actuator to open the door by disengaging the "clamshell" from the door spring assembly.

7.3.2.1.2 Unprotected Control Register

The unprotected control register contains control bits that cannot directly cause damage the FUV detector. The control bits allocated to this register are as follows:
HV power - Turns on/off HV power.
HV grid – Turns on/off the HV grid power.
Door motor direction – Two-Bit value to define door direction: 0=Stop, 1=Open, 2=Close.
Door motor power - Turns on/off power to the door motor.

7.3.2.2 HVPS Digital-to-Analog Converter (DAC)

The DCE FSW uses the High-Voltage Power Supply (HVPS) Digital-to-Analog Converter (DAC) to control the HVPS. The DAC converts a digital value to a low-voltage (0 to +5 volts) value, which is then converted in hardware to a high-voltage value in the approximate range of -2000 to -6000 volts at the detector head.

The DCE FSW uses the DAC to command the HVPS to a new voltage level and to set the maximum voltage level. Status information concerning the state of the HVPS is returned to the FSW via the multiplexer (MUX) and Analog-to-Digital Converter (ADC).

7.3.2.3 Digitizer 3-Wire Interface

The digitizer is the electronics that interprets photon events. The criterion used to qualify an event can be controlled via commands. The digitizers commands are sent via a synchronous serial link implemented with 8051 port pins. The digitizer returns setting talk-backs as an input to the MUX/ADC. The digitizer is programmed with default values upon power-on reset, and after that, settings are modified only on command.

The DCE FSW uses a 3-wire interface to send commands to the digitizer hardware. The DCE FSW sends values that set event filtering values among other adjustment values for controlling digitizer performance. The FSW sends over digital values that are converted to analog values by the digitizer.

7.3.2.4 Analog-to-Digital Converter (ADC)

An analog-to-digital converter (ADC) converts sensor voltages to digital values that are stored in the housekeeping data area. The sensors can collect temperature, voltage or current information, and hardware talk-back information.

The FSW must use the multiplexer (MUX) to select the appropriate ADC input source and to tell the ADC to perform the conversion. After selecting the desired source and initiating the conversion, the FSW must wait a short time for the input to settle. After waiting the settle time (approx. 60 microseconds per sensor), the FSW reads the ADC converted value and stores it in the appropriate housekeeping location.

Certain ADC inputs (e.g. High Voltage and Auxillary Current) must be gathered at the high rate of approx. once per 4 milliseconds, while all other ADC inputs are read approx. once per second.

7.3.2.5 Multiplexer (MUX)

As described in the ADC section, the multiplexer is used to select the appropriate input to the analog-to-digital converter. There are a number of possible ADC inputs that can be selected using the MUX.

In addition to selecting ADC inputs by writing to the MUX address, the same address is used to gather status information about the door and high-voltage. The state of the door and high-voltage can be determined by reading the MUX address. It should be noted that the DCE FSW is not reading from the MUX but rather from another latch that has the same address as the MUX. Some of the status bits reflect whether HV and grid have been powered on, and door switches (latched, opened and closed).

7.3.2.6 Counters

Counters reflect the number of photon events that have passed through the various stages of the digitizing process. There are several types of counters that count specific types of events. The FUV hardware has three types of counters: front end counters (FECA & FECB), digitized event counters (DECA & DECB), and science data counters (SDC1 & SDC2).

Each counter counts only the photon events that meet some criterion specified by the digitizer and its threshold settings. The count rate protection software uses the FEC counters to determine when a global count rate violation has occurred. Each type of counter has an A & B counter that maps to each FUV detector segment.

7.3.2.7 Pulse Height Histograms

Pulse Height (PH) Histogram data consists of 256 bins (128 per each of the two detector segments) of consecutive 16-bit words. This data represent the total number of photons that were detected and distributed into bins according to their pulse-height as determined by the digitizer hardware.

The FSW periodically reads the PH bins and outputs that information to the CS through housekeeping. The act of reading the PH data causes the bins to be reset to zero.

The memory used to store PH data is accessible to both the PH Counter hardware and the 8051. An attempt to simultaneously access the same memory by both the 8051 and the PH Counter hardware could result in corrupted data. The PH Counter hardware design requires the 8051 to assert a PH disable signal while accessing the PH Counter memory and de-assert the signal when done.

7.4 OPERATING MODES

This section examines the two DCE FSW operating modes: Boot and Operate. It describes the functionality the operating modes provide and how the user transitions from one mode to another.

The DCE FSW is composed of two related software executables known as the Boot code image, and the Operate code image. The Boot code image is burned into PROM and cannot be changed once the COS instrument is on-orbit. The Operate code image is stored outside the DCE and loaded into DCE RAM via the DCE's upload command.

7.4.1 Boot Mode

The DCE embedded processor begins execution of the Boot flight software contained in PROM whenever power is applied to the FUV Detector Subsystem or when a reset occurs. The primary purpose of the Boot software is to provide a robust, non-volatile code image from which to load the Operate code images into RAM. Once the DCE is in Boot mode, the ground can then send commands to put the FUV Detector Subsystem into an operational state.

The Boot code provides enough capabilities to upload an Operate code image and transfer microprocessor control to the Operate code. This allows the Operate code image to be actively managed on the ground and new versions to be uploaded to the FUV detector. The Boot code also allows memory tests to be performed on the Operate code areas in 32K RAM area since Boot runs out of PROM.

The Boot code provides a subset of the capabilities found in the Operate code. The following is a list of Boot code capabilities:

- Perform initialization functions, including reset tests and memory initialization.
- Command reception and processing
- Housekeeping data reporting including memory monitors
- Memory uploads into DCE RAM
- Memory dumps from DCE memory
- Begin execution of the Operate code image
- Processing of a subset of DCE commands (but no HV, door or digitizer commands)
- Background CRC checking and stack monitoring

Since Boot does not support any HV, door or digitizer commanding, there is no need for count rate protection or current limit protection capabilities in the BOOT Code image.

7.4.2 Operate Mode

Operate mode is entered after a DCE Operate code image has been loaded into DCE memory and the DCE has received a jump-to-operate command. After receiving the jump-to-operate command, the Boot code transfers control to the Operate code image.

The Operate code provides a superset of FUV detector control capabilities. The following is a list of Operate code capabilities:

- Command reception and processing
- Housekeeping data reporting including memory monitors
- Memory uploads into DCE RAM
- Memory dumps from DCE memory
- Processing of all DCE commands including HV, door and digitizer commands
- Ramp detector high-voltage
- Current limit protection
- Count rate protection
- Move the door mechanism
- Background CRC checking and stack monitoring

7.4.3 Mode Transitions

As described above, Boot code begins executing as the result of power being applied to the FUV detector electronics or due to a microprocessor reset. While in BOOT mode, an Operate code image can be uploaded into DCE RAM. Once the OPERATE image is successfully copied, the jump to operate command can be sent to transfer control to the Operate code. This is the standard process for transitioning between Boot and Operate modes.

Boot mode can be entered under the following conditions:

- a power-on reset occurs
- a watchdog timer reset occurs while in Boot mode
- a reset command was received and processed by the Boot mode software
- a watchdog timer reset occurs while in Operate mode
- a reset command was received and processed by the Operate mode software

Operate mode can be entered under the following conditions:
a jump-to-Operate command was received and processed while executing in Boot mode

7.5 SOFTWARE ARCHITECTURE

This section addresses the physical software components that make up the DCE FSW. In the DCE FSW there are four major software component types: initialization code, an executive loop, interrupt service routines, and tasks. Each type of component is discussed in the following sections. Before looking at the major software components individually, a discussion of the operating system is necessary.

7.5.1 Operating System

The DCE flight software does not use a commercial off-the-shelf (COTS) operating system (OS). The operating system is built from the ground up using a simple design. The DCE FSW operating system consists of an executive loop that invokes a series of functions in a round-robin fashion along with interrupts that provide pre-emptive processing. The functions invoked by the executive loop and ISRs are called tasks. Each task provides a unique set of functionality to the DCE FSW. Each of these tasks is described in greater detail in following sections.

7.5.2 Resets and Initialization

The DCE can be reset for a variety of reasons. A reset occurs whenever power is applied to the DCE, or whenever the watchdog timer has not been stroked quickly enough. Each of these resets causes the DCE FSW to start executing from its PROM. This section examines the resets that can occur in the system and how the DCE FSW initializes itself as a result of the various resets.

FUV detector initialization consists of the steps the DCE FSW must go through to properly setup its operating environment. Initialization steps include configuring the various pieces of DCE hardware, initializing global memory areas and starting execution of the various tasks in the system. This section covers the DCE FSW requirements that deal with resetting the system and causing the DCE FSW to re-initialize.

7.5.2.1 Power-On Reset

A power-on reset (POR) is treated as if the hardware has just been powered on. While this kind of reset is intended to be used only during an actual power-on event, it is also a commandable event that forces the DCE into a default, known state. A power-on reset causes a complete initialization of the software to occur.

7.5.2.2 Watchdog Reset

A watchdog reset occurs when the watchdog timer has not been "stroked" (i.e. reset) often enough. If the watchdog count down timer reaches zero before being reset, a watchdog timer reset occurs. This type of reset can be due to a single event upset (SEU), a coding error, or some spurious event. Just like the POR, a watchdog timer reset can be commanded from the ground.

This is a catchall-type reset that is named for its most likely cause: the 8051 built-in watchdog reset timer, which can cause the 8051 to jump to its reset vector. This type of reset assumes that power had been previously applied to the DCE. A watchdog reset causes a minimal initialization of the software to occur.

7.5.2.3 Commanded Resets

A commanded reset occurs as a result of a reset command being sent to the DCE FSW from the CS. There are four possible ways to command the DCE FSW to reset the DCE. Two of the commands result in complete reset of the DCE FSW, and the other two result in a minimal initialization. The four ways to command DCE reset include:

- The CS can reset the DCE by toggling the DCE hardware reset line. This does not result in a command being sent to the DCE FSW. This reset command results in the DCE FSW executing its minimal initialization sequence.

- The CS sends an Initiate Watchdog Reset command to the DCE. This reset command results in the DCE FSW executing a minimal initialization sequence.
- The CS sends a single command word that contains the value 0x80000000. This reset command results in the DCE FSW executing a complete initialization sequence.
- The CS sends an Initiate Power-On Reset command to the DCE. This reset command results in the DCE FSW executing a complete initialization sequence. (NOTE: The DCE forces the complete initialization sequence to run by scrambling a fixed bit pattern in memory to make it appear as if a powered up of the DCE occurred.)

7.5.2.3.1 Reset Summary Table

Source of Reset	**Initialization Sequence Executed by FSW**
Power-on Reset: power is applied to the DCE hardware	Complete Initialization Sequence
Watchdog Reset: Watchdog timer expires	Minimal Initialization Sequence
Commanded Reset #1: CS sends a command to perform a complete initialization (aka Initiate Power-On Reset command)	Complete Initialization Sequence
Commanded Reset #2: CS sends a command word containing 0x80000000	Complete Initialization Sequence
Commanded Reset #3: CS toggles DCE hardware reset line	Minimal Initialization Sequence
Commanded Reset #4: CS sends a command to perform a minimal initialization (aka Initiate Watchdog Reset command)	Minimal Initialization Sequence

7.5.2.4 Initialization Sequence

The following bullet list descrbes, in general terms, the initialzation sequence for the DCE FSW. Note, this sequence is identical for both the Minimal and Complete Initialization – except for the step involving the patachable constants table. (See the step labled ‘Check Reset Type’ below.)

Initialize the 8051 Processor
Disable all Interrupts
Stop Timers
Reset Stack to Base Level
Disable the Programmable Counter Array (PCA) Watchdog Timer

Safe the FUV Hardware
    Set 8051 to Default State

HV OFF
Door OFF
Stims OFF)
Clear appropriate Internal and External Memory
Check for Reset Type
If Watchdog Reset (i.e., Minimal Initialization Sequence)
Issue Diag 1c
If Power-On Reset: (i.e., Complete Initialization Sequence)
Copy Default Patchable Constants from PROM to RAM
Issue Diag 1b
Setup Interrupts
Setup Standard 8051 Timers
Setup Primary Command Interface
Setup Secondary Command Interface
Start Background CRC Calculations
Setup for Housekeeping Packet Construction

7.5.3 Interrupt Service Routines

Interrupt service routines provide pre-emptive processing in the DCE FSW. Since the operating system consists of a round-robin loop that executes tasks in a pre-determined order, only interrupts can provide pre-emptive processing. The DCE FSW supports two interrupts: the timer interrupt and the command traffic interrupt. This section describes the interrupt service routine (ISR) associated with each interrupt.

7.5.3.1 Timer ISR

The timer interrupt is physically linked to the 8051 timer hardware. The timer hardware is programmed to "tick" approximately 50 times per second in BOOT mode and 250 times per second in OPERATE Mode.

The timer interrupt triggers the Timer ISR to execute. The ISR sets flags used by some tasks to control timing behavior. The Timer ISR keeps track of the number of times it is invoked, and maintains several software timers as a result. The software timers are used to control the following activities:

Invocation of the Current Limit Protection (CLP) Task (approx. every 4 milliseconds)
Invocation of the HV Ramp Task (approx. every 0.1 second)
Invocation of the Count Rate Protection (CRP) Task (approx. every 1 second)
Invocation of the Door Protection Task (approx. every 1 second)
Collection of Counters A & B data (approx. every 1 second)

Reading of Analog sensor data (approx. every 1 second)

7.5.3.2 Command ISR

A command interrupt goes off when a 32-bit command word has been placed into the set of four 8-bit command registers. The DCE has two sets of command registers with an interrupt for each set. This interrupt causes the Command ISR to execute. (See Section 7.3.1.1)

The main function of the ISR is to move data into memory for processing by the Process Command Task. As command words are received, they are processed by this ISR. The command words are written into RAM in the Command Buffer region based on the address information contained in the command word. After all of the command words for a particular command are received, the Process Command Task processes the command.

This ISR also provides a means of resetting the software if the executive loop should hang for any reason. Any command word that consists of a one in the most significant bit with zeros in all other bits causes the ISR to command a reset of the DCE.

7.5.4 Tasks

This section describes the various tasks that comprise the DCE flight software.

7.5.4.1 Process Command Task

The DCE FSW provides a method for the successful and timely reception and interpretation of command packets from the outside world. The Process Command Task is responsible for processing all commands entering the DCE subsystem. Commands are received from the outside world on an approx. once-per-second basis.

The Command ISR accepts command words and upload data and stores the information in the Command Buffer region of RAM. Once there, the Process Command Task can process the command packet.

The task first checks for a valid command format. If the command is valid, it is executed. The task copies the contents of the Command Buffer to an area in the housekeeping region, thus preserving the parameters for use by the command. It also provides a command echo in housekeeping.

Executing the command means the Process Command Task calls the appropriate command function. (See FUV ICD, Appendix D and/or DM-05 Appendix B for a

complete list of available DCE Comands.) When the DCE is in Boot mode, only a subset of all DCE commands can be executed. More specifically, all commands are available in Boot except for the commands that enable hardware functions to the HV, Door and Digitizers and those commands to configure the protection tasks for the HV and the Door.

The Process Command Task also sets a flag used by the Housekeeping Task to indicate that a housekeeping response is required. Every command op-code, valid or not, elicits a response from the DCE. If the command is invalid and not executed, the DCE reports the attempt in housekeeping. The command response may be interpreted as readiness for a new command packet at the DCE. A housekeeping packet contains enough information to determine whether the command packet was executed properly. The task may also produce a housekeeping packet that contains download data in response to a download command.

When the task returns control to the executive loop, it is always in the same state. It is always searching for the presence of a command op-code.

The Process Command Task has no DCE commands associated with it that cause it to perform different types of processing. The Process Command Task is responsible for processing all commands and invoking the appropriate command function, however, none of those command functions alter its behavior.

7.5.4.2 Read Sensor, Build & Send Housekeeping and Dump Packet Tasks

The Sensor, Housekeeping and Dump Tasks are responsible for collecting counter information, collecting hardware and software status, and sending out housekeeping and dump packet. The Read Sensor Task collects analog sensor information once per second, while the Build and Send Housekeeping Packet Tasks collects this and other housekeeping information and sends out the housekeeping packet. The Dump Packet Task sends out a dump packet, if one has been requested by a Dump command.

When all of the housekeeping information is collected, the Send Houseking Task sends the housekeeping packet across the Command/Housekeeping interface. The packet consists of 512 32-bit housekeeping words. The housekeeping words are written sequentially to a set of four 8-bit registers. (See Section 7.3.1.2)

7.5.4.3 Background CRC Task

The Background CRC Task computes a 16-bit cyclic redundancy check (CRC) value that characterizes a defined region of DCE memory. The task reports changes in a memory region when the newly computed CRC for that region differs from the previously

computed value. This task reports changes as diagnostic messages and does not attempt to correct any memory errors.

This task is a background task and does not attempt to calculate the CRC for an entire region each time it is invoked. However, it will continue to processes one byte of data at a time through the CRC algorithm until it has either completed the current memory region or until it is interrupted by another task. After the CRC for a memory region has been computed, the task checks to see that the value matches the CRC value stored in memory. If the values differ, the task reports a diagnostic and stores the newly computed CRC in housekeeping.

The following two tables give CRC Region Information and Expected CRC values for BOOT and OPERATE Code.

BOOT Code CRC Regions

Region	**Address Range**	**Expected CRC Value**
00 – Commanded CRC	Defined by User Command	N/A
01 – First 6k of PROM	0x0000 – 0x17FF	0xC001
02 – Remaining 2k of PROM	0x1800 – 0x1FFF	0xC001
03 – RAM – 4k	0x8000 – 0x8FFF	0x0FE1
04 – RAM – 4k	0x9000 – 0x9FFF	0x0FE1
05 – RAM – 4k	0xA000 – 0xAFFF	0x0FE1
06 – RAM – 4k	0xB000 – 0xBFFF	0x0FE1
07 – RAM – 4k	0xC000 – 0xCFFF	0x0FE1
08 – RAM – 4k	0xD000 – 0xDFFF	0x0FE1
09 – RAM – 4k	0xE000 – 0xEFFF	0x0FE1
10 – RAM – 4k	0xF000 – 0xFFFF	0x0FE1

OPERATE Code CRC Regions

Region	**Address Range**	**Expected CRC Value**
00 – Commanded CRC	Defined by User Command	N/A
01 – First 6k of PROM	0x0000 – 0x17FF	0xC001
02 – Remaining 2k of PROM	0x1800 – 0x1FFF	0xC001
03 – RAM – 2k	0x8800 – 0x8FFF	0xC0DE
04 – RAM – 2k	0x9000 – 0x97FF	0xC0DE
05 – RAM – 4k	0x9800 – 0xA7FF	0xC0DE
06 – RAM – 2k	0xA800 – 0xAFFF	0xC0DE
07 – RAM – 2k	0xB000 – 0xB7FF	0xC0DE
08 – RAM – 4k	0xB800 – 0xC7FF	0xC0DE

The task is initialized to point to the first memory region in a list of memory regions to be checked. In general, the task completes its check of a region and automatically starts computation of the next region in the list. After all regions in the list have been checked, it starts back at the beginning of the list.

The Compute CRC command causes the CRC Task to stop its current CRC calculation and start a new one. This command causes the CRC Task to calculate a CRC for a user-specified range of DCE memory. Once that CRC value is calculated, the task re-initializes itself and starts checking from the first memory region in the list.

7.5.4.4 Current Limit Protection Task

The Current Limit Protection (CLP) Task checks the HV and Aux current readings for over-limit conditions. It reads the current values, records the information as data samples, and determines if an over-limit condition occurred. In the event of an over-limit, the task reports a diagnostic and turns off HV, if warranted.

This task runs as fast as possible to monitor the power current levels – without disrupting the ability of the DCE FSW to perform it's other tasks. Thus, the CLP task executes approx. once every 4 millisedons. It saves the last 1024 currents samples in RAM so that they can be downloaded for analysis if necessary. This task is capable of reporting HV over current events without turning off the HV. It is also capable of recognizing a sustained over-limit condition. If the current level remains out of limits over a specified persistence interval, the task shuts off the HV and reports the over-limit event in housekeeping.

If a single over-limit event is detected, this task reports a diagnostic. Subsequent over-limit samples are counted but no diagnostic is posted until the consecutive out-of-limits count is reached. If a current value within limits is read, the consecutive out-of-limits counter is reset to zero. When the consecutive out-of-limits count is met or exceeded, this task turns off power to the HV supply.

Default parameters for the Current Limit Protection Task are loaded during power-on reset initialization. The parameters can then be modified via DCE commands.

7.5.4.5 Count Rate Protection Task

The Count Rate Protection (CRP) Task checks the digitizer counters (FECA and FECB) on a once per second basis for excessive counts. Every second the CRP Task stores these count values in a rotating buffer in DCE Memory, and performs an average of these stored values. If the average value of this buffer meets or exceeds the specified count rate limit, the CRP Task forces the HV to the minimum of either it's present voltage, or

the HV_LOW state voltage. (In short, this task performs a "moving average" of the FEC counters – and will drop the voltage to HV_LOW if the "moving average" meets or exceeds the specified limit.) If the HV ramping is active when a CRP limit violation occurs, the ramping will stop.

Default parameters for the Count Rate Protection Task are loaded during power-on reset initialization. The parameters can then be modified via DCE commands.

7.5.4.6 High Voltage Ramping Task

The High Voltage Ramping Task is responsible for increasing the MCP voltage on the detector in small increments. When ramping the detector, the task starts at the current HV level and increments the voltage until it reaches the commanded nominal HV value. The HV ramp rate is used to pause for a set amount of time between successive HV commands.

Before the HV ramping can begin, the DCE FSW must first be commanded to setup internal parameters used in the ramping process: the low HV value, the nominal HV value, and the HV ramp rate. The ground must also set the maximum voltage level (HV MAX) enforced by the hardware. This ensures that the flight software cannot command the high voltage to a level higher than the maximum level allowed by the hardware.

With the configuration complete, high voltage ramping can being. The task uses the previously set parameters to determine how to perform the ramping. The task writes to the HV DAC registers to command small increments in high voltage. After each DAC command, the task waits for the specified 'ramp' time before further incrementing the HV DAC registers. This process continues until the HV has reached the requested HV value. The task does not change the HV MAX register.

The High Voltage Ramping Task maintains a task state variable, and two ramping bits that indicate whether ramping is in progress or not.

Default parameters for HV Ramping Task are loaded during power-on reset initialization. The parameters can then be modified via DCE commands.

7.5.4.7 Door Protection Task

The Door Task performs periodic checks of the auxillary current, the door timer and the actuator latch. If the condition warrants, this task performs a Door Stop. The task performs three basic functions. It monitors the auxillary current to see if it meets or exceeds a specified limit for three or more telemetry updates, it monitors a "3-minute"

door timer to see if the timer has elapsed, and it monitors the actuator latch to see if it has changed states.

Once a second the door task decrements the door "3-minute" timer, and checks to see if the timer has expired. If it has, a Door Stop is performed. If the timer has not expired, the task checks the Aux current against a specified limit. If the Aux current is out of limit for three or more consecutive samples, a diagnostic message is reported and a Door Stop is performed. The task also monitors the actuator latch state to see if it has changed states. If the task detects a state change for the latch, it changes the door timer value to 2 seconds – so that 2 seconds later the timer will expire and a Door Stop will be performed. A Door Stop consists of turning off door motor power, turning off actuator power, disabling the door motor and actuator enables, setting the door direction to 'stop', clearing the door motor override, and resetting the door motor timer to zero.

Default parameters for the Door Protection Task are loaded during power-on reset initialization. The parameters can then be modified via DCE commands.

8. HARDWARE/SOFTWARE INTERFACE INFORMATION

This section gives the overall memory map, the memory mapped read registers, with the bitwise format of each, the write registers and the internal 8051 ports.

8.1 DCE PROCESSOR MEMORY MAP

The DCE 8051 microcontroller, like all 8051 variants, reads instructions from external memory. Utilizing 16-bit addresses for code, up to 64KB may be accessed. Similarly, it may access up to 64 KB of external data memory (RAM). The Harvard Architecture of the machine means that these two 64 KB spaces are separate. By physically tying the CODE read line to the DATA read line, external instructions and external data may be drawn from the same physical device (Von Neumann Architecture). The table below shows how external memory is utilized by the DCE 8051. Note that a Harvard architecture is employed below the 32 KB boundary and Von Neumann architecture employed above that. Note also that no external RAM exists in the range 4000-7FFF – this 16 KB being reserved for memory-mapped I/O.

Address (Start of Segment)	CODE Space	External Data Space
0000h	BOOT Mode Reset Vector	unused
0003h	BOOT External 0 Interrupt Vector	
000Bh	BOOT Timer 0 Interrupt Vector	
0013h	BOOT External 1 Interrupt Vector	

Address (Start of Segment)	CODE Space	External Data Space
001Bh	BOOT Timer 1 Interrupt Vector	
0023h	BOOT Serial Port Interrupt Vector	
002Bh	BOOT Timer 2 Interrupt Vector	
0033h	BOOT PCA Timer Interrupt Vector	
0040h	BOOT Code	OPERATE Mode Upload Data
0440h		OPERATE Mode Command Packet
045Ch		unused
1040h		OPERATE Mode Download Data
1440h		OPERATE Mode Housekeeping Packet
1840h		unused
2040h		BOOT Mode Upload Data
2440h		BOOT Mode Command Packet
245Ch		BOOT Mode Patchable Constants
3040h		BOOT Mode Download Data
3440h		BOOT Mode Housekeeping Packet
3840h		unused
3FFAh		Reset Memory Pattern
4000H	Not physically present	Memory Mapped I/O
8000h	OPERATE Mode Entry Vector	
8003h	OPERATE External 0 Interrupt Vector	
800Bh	OPERATE Timer 0 Interrupt Vector	
8013h	OPERATE External 1 Interrupt Vector	
801Bh	OPERATE Timer 1 Interrupt Vector	
8023h	OPERATE Serial Port Interrupt Vector	
802Bh	OPERATE Timer 2 Interrupt Vector	
8033h	OPERATE PCA Timer Interrupt Vector	
8040h	OPERATE Code, Patchable Constants and Data	
FFFFh	end of memory	

Concerning the above memory map,

1. Code space 0000-3FFF (16 KB) is provided by two 8 KB PROM chips.
2. No physical memory device resides in Code space 4000-7FFF (16 KB).
3. Data space 0000-3FFF (16 KB) is provided by a 32 KB RAM chip, only half of which is utilized. Pin P1.6 on the 8051 switches between the upper and lower halves of this RAM chip, but this feature is not implemented in software (i.e., P1.6 is left in its default reset state of '1').
4. Data space 4000-7FFF is reserved for memory-mapped I/O. This is far more than is necessary, but the Data space was not needed for RAM and it makes for simpler address decoding in the hardware design.
5. Code and Data space 8000-FFFF is provided by one 32 KB RAM chip. A Von Neumann architecture is employed for this range of addresses.
6. Utilization of Code space addresses 0000-0036 as the reset and ISR vectors is imposed on the design by 8051 architecture. Because these addresses reside in PROM and yet must accommodate the interrupt service routines of both Boot and Operate modes, special handshaking is necessary. The Operate mode entry and ISR vectors found at addresses 8000-8036 are part of this handshaking.
7. Operate mode RAM usage in ranges 0040-045B and 1040-183F is imposed on the DCE by its interface to the CS computer.
8. Boot mode RAM usage in the range 2040-383F is imposed on the DCE by its interface with Operate mode. This memory range was selected because it mirrored the Operate mode range 0040-183F but did not overwrite any Operate-mode data.
9. The 6-byte Reset Memory Pattern located in RAM at 3FFA-3FFF allows the Boot mode to determine the type of reset which occurred – power-on reset or watchdog reset.

8.2 MEMORY MAPPED READ REGISTERS

The DCE hardware provides memory mapping to all necessary counters and hardware talkbacks. These include various event counters, pulse-height histogram counters, digitized voltage and temperature readings, bilevel status words, and command input.

8.2.1 Counters A and B

Counters reflect the number of photon events that have passed through the various stages of the digitizing process. The FUV hardware has three types of counters: front end counters (FECA & FECB), digitized event counters (DECA & DECB), and science data counters (SDC1 & SDC2). All counters are 3 byte quantities and are read-only. Reading the most-significant byte (MSB) of a counter clears its contents.

Counter	Addresses (hex)		
	MSB		LSB
FECA	6002	6001	6000
DECA	6006	6005	6004
SDC1	600A	6009	6008
FECB	6102	6101	6100
DECB	6106	6105	6104
SDC2	610A	6109	6108

8.2.2 Pulse-Height A & B Status

Segment A and B pulse height histograms are designated PHA and PHB, respectively. Each segment occupies 256 consecutive bytes of address space – 128 2-byte bins logically grouped as 4 32-bin "slices" per segment. The 2-byte bin counters are little-endian (LSB in the lower address). Reading the PH data does not clear it. This must be performed in software by writing zeros (the memory is read/write accessible). Since the PH counters are accessed by the digitizers as well as the DCE, a locking arrangement prevents contention. In order for the digitizers to have access to increment the PH data, the PH Disable line must be cleared (8051 port pin P1.5 = '0') The DCE may read and write to this memory by first setting the PH Disable line (P1.5 = '1'), and then must clear P1.5 = '0' afterward to return control to the digitizer hardware.

PH Segment		Address Range (hex)
Segment A	Slice 0	6200 – 623F
	Slice 1	6240 – 627F
	Slice 2	6280 – 62BF
	Slice 3	62C0 – 62FF
Segment B	Slice 0	6300 – 633F
	Slice 1	6340 – 637F
	Slice 2	6380 – 63BF
	Slice 3	63C0 – 63FF

8.2.3 Bilevel Status Information

Two bytes provide talkback information concerning hardware status. These are read-only registers. (Note: Address 4000h is used as a write address for A/D operations and should not be confused with the read address 4000h used by one of these bi-level talkback registers.)

Address (hex)	Bit	Description
4000 (bit 0 is LSb)	0	'1' = Door Latched
	1	'1' = Door Open
	2	'1' = Door Closed
	3	'1' = High Voltage On
	4	'1' = High Voltage A/B enabled (at Safe Plug)
	5	'1' = High Voltage Filter Module (at Safe Plug)
	6	'1' = High Voltage Enabled (Safe Plug is in)
	7	Detector Identification bit 0
4500 (bit 0 is LSb)	0	'1' = Auxillary Power Enabled
	1	'1' = Actuator Enabled
	2	'1' = Motor Enabled
	3	'1' = Motor Enable On
	4	'1' = Auxillary Power On
	5	HV0 Status ('1' = HV DAV voltage near zero, OK to enable HV)
	6	'1' = Door Enabled (Safe Plug is in)
	7	Detector Identification bit 1

8.2.4 ADC Digitized Temperature, Voltage, and Current Readings

An analog-to-digital converter (ADC) converts sensor voltages to digital values that are stored in the housekeeping data area. The sensors collect temperature, voltage and current information, among other things. This ADC is multiplexed within the DCE so that 40 analog channels are available. In order to take a particular reading, the FSW must write the 1-byte address of the device to the MUX (address 4000h), delay while the analog value settles at the input to the ADC (~50 _s), command the ADC to take a

reading (write any 1-byte value to address 4700h), delay for the A/D conversion process (~10 _s), and finally read the 1-byte value from the ADC (address 4700h). The 40 available sensors are described below.

MUX Address (hex)	Mnemonic	Description
08	LFTDVAA	Detector 1 Temperature
09	LFTACT	Actuator Temperature
0A	LFTHVFM	Filter Module Temperature
0B	LFTHVPS	High Voltage Temperature
0C	LFTTDCA	TDC-A X Temperature
0D	LFTIP	Ion Pump Temperature
0E	LFTAMPA	Amplifier A Temperature
0F	LFTAMPB	Amplifier B Temperature
10	LFTTDCB	TDC-B X Temperature
11	LFTDVAB	Detector 2 Temperature
12	LFTLVPC	LVPS Temperature
13	LFTDCE	DCE-B Temperature
14	LFTFAN	F Status
15	LFVP5DC	+5 Volt Supply (scaled down by 1.25)
16	LFVP15D	+15 Volt Supply (scaled down by 3.75)
17	LFVM15D	-15 Volt Supply (scaled down by 3.75)
20	LFRPOS	Door Position
21	LFRAXI	LVPS Auxillary Current Monitor
22	LFHIMONA	HV-A Current Monitor
23	LFHIMONB	HV-B Current Monitor
24	LFHVMONA	HV-A Monitor
25	LFHVMONB	HV-B Monitor
26	LFHQANA	Q Status A

MUX Address (hex)	Mnemonic	Description
27	LFHQANB	Q Status B
40	LFRAXAN	Auxillary Status
41	LFRMTRAN	Motor Status
42	LFRACTAN	Actuator Status
43	LFVPMON	LVPS Power Monitor
44	LFHVSETA	HV-A Programming Voltage
45	LFHVSETB	HV-B Programming Voltage
46		TDC-A (portal to TDC-A MUX addresses)
47		unused
80	LFVP5DA	+5 Volt Monitor from DCE-A
81	LFVP5DB	+5 Volt Monitor from DCE-B
82		TDC-B (portal to TDC-B MUX addresses)
83		unused
84	LFHVMAXA	HV-Max-A Programming Voltage
85	LFHVMAXB	HV-Max-B Programming Voltage
86		Gnd
87		Gnd

Multiplexer address 46h provides access to digitizer A (TDC-A) hardware and MUX address 82h provides access to digitizer B (TDC-B). Each digitizer has 12 channels of D/A output and 17 channels of A/D input (12 talkbacks from the D/A outputs plus 5 TDC voltage readings). In order to read an analog value from a TDC, one must first write the TDC MUX address to the TDC (A or B) then perform a regular ADC reading using the correspoinding portal MUX address (46h or 82h).

Writes to the TDCs (for both DAC and ADC purposes) are performed serially, requiring that 16 bits be clocked out to the device (MS-bit first). The physical interface between the 8051 and the TDC is a 3-wire link: Clock, Data, and Enable. The Clock and Data

lines are shared by both TDCs ‘A’ and ‘B’, but each, necessarily, has its own Enable line. To clock 16 bits to a TDC, the following sequence is performed:

1. Clock = 0
2. Enable = 1
3. Set the Data line with the next data bit
4. Clock = 1 (this clocks the bit into the TDC)
5. Wait at least 1.5 _s
6. Clock = 0
7. Loop to step 3 until all 16 bits are sent
8. Enable = 0 (i.e., disable the TDC’s communications with the DCE)

The DCE 8051 port bits corresponding to these control lines are:

Control Line	8051 port bit
Clock	P1.0
Data	P1.1
TDC ‘A’ Enable	P1.2
TDC ‘B’ Enable	P1.3

In the case of an ADC reading, the lower 8 bits are discarded by the TDC (but must be sent to complete the hardware clocking). For DAC commanding, the lower 8 bits are the data value being sent. Hardware addresses for the TDC’s 12 DAC and 17 ADC channels are shown in the following table. These addresses form the upper 8 bits of the 16-bit value sent to the TDC.

TDC Address (hex)	Mnemonic	Description
10		DAC Shift X
11		DAC Stretch X
12		DAC Begin Walk X
13		DAC End Walk X
20		DAC Timing Threshold Y

TDC Address (hex)	Mnemonic	Description
21		DAC Lower Charge Threshold
22		DAC Upper Charge Threshold
23		DAC Timing Threshold X
30		DAC Shift Y
31		DAC Stretch Y
32		DAC Begin Walk Y
33		DAC End Walk Y
40	LFGSHFAX	ADC Shift X
41	LFGSTRAX	ADC Stretch X
42	LFGBWKAX	ADC Begin Walk X
43	LFGEWKAX	ADC End Walk X
44	LFGTTAY	ADC Timing Threshold Y
45	LFGLQTA	ADC Lower Charge Threshold
46	LFGUQTA	ADC Upper Charge Threshold
47	LFGTTAX	ADC Timing Threshold X
50	LFVP15TA	ADC +15 Volt Supply
51	LFVM15TA	ADC -15 Volt Supply
52	LFVP5TA	ADC Vcc
53	LFVM5TA	ADC -5.2 Volt Supply
54	LFGREFA	ADC Vref
60	LFGSHFAY	ADC Shift Y
61	LFGSTRAY	ADC Stretch Y
62	LFGBWKAY	ADC Begin Walk Y
63	LFGEWKAY	ADC End Walk Y

8.2.5 Rx registers

Communication from the CS to the DCE microcontroller is performed over redundant 1 MHz synchronous serial links. Hardware handles all transfers, including toggling of handshake "busy" lines and interrupting of the processor when data is received. All data (including commands) consists of 32-bit long words, the upper 16 bits of which form the address and the lower 16 bits being the data for the word. The data word is stored little-endian in the DCE memory (i.e., the "Data LSB" is stored at the specified 16-bit address and the "Data MSB" is at the next higher byte address).

32-bit Data Word Hardware Read Addresses (hex)				
Command Channel	Address MSB	Address LSB	Data MSB	Data LSB
Primary	5300	5200	5100	5000
Secondary	5700	5600	5500	5400

For redundancy, data is sent from the CS to the DCE via either the primary or secondary command channel. Upon receipt of a data word on the primary command channel, the shift register hardware pulls the DCE (8051) EX0 interrupt line to a low state. The interrupt on this channel should be level-triggered. Similarly, the secondary command channel hardware pulls the EX1 interrupt line to a low state upon receipt of a command long word. The ISRs associated with these interrupts must read the 4 data bytes from the hardware addresses given in the above table, reading the "Data LSB" last since doing so clears the hardware "busy" line and allows the CS computer to send the next 32-bit word.

8.3 MEMORY MAPPED WRITE REGISTERS

The DCE hardware provides memory mapping to various control registers and Digital-to-Analog Converters (DACs) which allow complete control of the High-Voltage Power Supplies (HVPS) and door motion. Additionally, memory mapped I/O is used for sending data words from the DCE to the CS computer.

8.3.1 Protected Control Register

The protected control register – address 4300 – is read/write accessible. Hardware schematics refer to this as "Controls2". In order to either read or write to the protected control register it must be unlocked by clearing 8051 port bit P1.4='0'. After accessing this register, relock it by setting P1.4='1'. This register is protected because severe degradation of the FUV detector may result if operated improperly. The bits in this register are detailed below.

Protected Control Register (address 4300) – "CONTROLS2"	
Bit (0=LS-bit)	Description
0	Auxillary Power Enable (1=Enable). The unprotected control register has a similar bit, either of which will enable auxillary power.
1	HOP Actuator 1 On (1=On)
2	HOP Actuator 2 On (1=On)
3	unused
4	Actuator(s) Enable (1=Enable)
5	unused
6	unused
7	Door Motor Override (1=Override)

8.3.2 Unprotected Control Register

The unprotected control register – address 4200 – is read/write accessible. Hardware schematics refer to this as "Controls1". No unlocking and locking are necessary to access this register. The bits in this register are detailed below.

Unprotected Control Register (address 4200) – "CONTROLS1"	
Bit (0=LS-bit)	Description
0	HV Enable. When this bit transitions from low-to-high, it clocks the hardware line HV0 to the HV enable line. HV0 is only high (true) if the current HV DAC setting is near zero, thus preventing HV enabling if the HV DAC is non-zero.
1	Grid Power (1=On)
2	Auxillary Power Enable (1=Enable). The protected control register has a similar bit, either of which will enable auxillary power.
3	Motor Direction. '00' = safe (off), '01' = Open, '10' = Close, '11' is disallowed.
4	
5	Motor Power (1=On)
6	unused
7	unused

8.3.3 HVPS Digital-to-Analog Converter (DAC)

The DCE FSW uses the High-Voltage Power Supply (HVPS) Digital-to-Analog Converter (DAC) to control the HVPS. The DAC converts an 8-bit digital value to a high-voltage value in the 2500 to 6500 VDC range at the detector head ('00'=2500 VDC, 'FF'=6500 VDC, linearly related). High voltage for both Segment 'A' and 'B' is controlled in this fashion. Further, for hardware protection, there are two 8-bit hardware registers associated with each segment: VMAX and VSET. Register 'VMAX' is set (by software) to the upper desired voltage setting and register 'VSET' is commanded to the desired voltage setting (again, by software). Hardware limits the actual DAC setting to the lesser of the VMAX and VSET outputs. Therefore, these registers are logically interchangeable in their purpose. The below table gives the hardware addresses for these write-only registers.

HVPS DAC Register Addresses (hex)	
Register	Address
VMAX, Segment 'A'	4400
VSET, Segment 'A'	4401
VMAX, Segment 'B'	4402
VSET, Segment 'B'	4403

Although these registers are write-only, status information concerning the state of the HVPS is returned to the FSW via the multiplexed Analog-to-Digital Converter (ADC).

8.3.4 Rx Registers

Communication from the DCE microcontroller to the CS is performed over a 1 MHz synchronous serial link which is identical to that used for commanding the DCE. Dedicated hardware handles the shifting of bits out of the DCE to the CS. All data consists of 32-bit long words, the upper 16 bits of which form the address and the lower 16 bits being the data for the word. The table below gives the hardware address to which to write each portion of the 32-bit word. The 'Address MSB' must be written last (address 5300), as writing to that hardware location initiates the bit transfer.

32-bit Data Word Hardware Write Addresses (hex)			
Address MSB	Address LSB	Data MSB	Data LSB
5300	5200	5100	5000

8.3.5 LED Display

For development and testing, a 9-segment LED bar display is mounted to the DCE-B board (near the 8051 microcontroller). All data writes to address range 2000-3FFF will be displayed on the lower 8 bits if the LED bar display.

8.4 THE 8051 MICROCONTROLLER – UT69RH051

8.4.1 UT69RH051 Implementation

The DCE 8051 microcontroller in use is the UT69RH051 variant. It is based on the 80C51FX microprocessor which is fully described in Chapter 5 of the document "MCS 51 Microcontroller Family User's Manual", dated February 1994. Radiation hardness features as well as implementation differences between the 80C51FX and the UT69RH051 variant are described in "UT69RH051 Radiation-Hardened Microcontroller Data Sheet", dated February 2000.

The UT69RH051 has 384 bytes of internal RAM, divided into three 128-byte groups. The first group is addressable both directly and indirectly using the address range 00-7F. This block holds the 4 8-byte register banks, 16 bytes of bit-addressable RAM, and other byte-addressable user RAM. The second group consists of byte-addressable user RAM which may only be accessed through indirect addressing to addresses 80-FF. The third block is the Special Function Registers (SFRs) which may only be accessed through direct addressing to addresses 80-FF. These SFRs include 4 bytes which directly map to the 4 8-bit ports on the 8051. Other SFRs include the stack pointer, data pointer for external memory access, accumulators, and registers which control the internal configuration of the 8051.

8.4.2 8051 Port Usage

In addition to memory-mapped I/O, the DCE 8051 microprocessor controls various hardware items through its available port pins. Various port pins are also used for input. The table below describes each such pin.

8051 Port Bits used for Direct Hardware Control		
Port Bit	Input/Output	Description
P1.0	Output	TDC Clock – data is clocked into the TDC on low-to-high transitions.
P1.1	Output	TDC Data
P1.2	Output	TDC ‘A’ Enable (1=enable)
P1.3	Output	TDC ‘B’ Enable (1=enable)
P1.4	Output	Locking bit for the protected control register, CONTROLS2 (1=protected).
P1.5	Output	Disable bit for the Pulse-Height data shared memory (1=disable ACTEL writes to PH shared memory so 8051 may access it).
P1.6	Output	RAM Bank Select. (1=use lower half of chip U8, 0=use upper half).
P1.7	Output	Reset for ACTEL “Counter”. A low pulse on this line (10 _sec minimum) will reset the ACTEL Counter FPGA. Returning the line to ‘1’ allows the ACTEL to start running.
P3.2	Input	Primary Command Interrupt. (0=hardware has received a full 32-bit word on its primary command channel)
P3.3	Input	Secondary Command Interrupt. (0=hardware has received a full 32-bit word on its secondary command channel)
P3.5	Output	8051 Reset. A low output on this line will force a reset of the 8051 microcontroller (which will restore this line to its high setting upon microcontroller reset). This also resets the ACTEL “CPU” FPGA.