

Date: Mon, 21 Feb 2000 17:00:00 -0800 (PST)
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To: rbrewster@hst.nasa.gov
Subject: COS info in text

Here's some text listings of the various addresses
and chip-selects within the COS DCE:

This is the address decoding scheme for the COS DCE-B Actel-CPU. Rev A
CODE SPACE (PSEN = 0 and PROM ON)
0000-7FFF PSEN code only CS_ROM~ ; read code from non-flight EPROM
0000-1FFF PSEN code only CS_ROM0~ ; read PROM 0
2000-3FFF PSEN code only CS_ROM1~ ; read PROM 1

(PSEN = don't care)

0000-FFFF RD or data or RD_RAM~ ; access Static RAM
PSEN code ; (write to SRAM using WR*)
new: 0000-3FFF RD or WR code CS_LowRAM~ ; 16k of extra data SRAM
(PROM OFF) ; for interrupt tables
8000-FFFF data or code CS_RAM~ ; access RAM (high)

DATA SPACE (PSEN = 1)

new: 0000-3FFF RD or WR CS_LowRAM~ ; 16k of extra data SRAM
(PROM ON)

2000-2FFF WR CS_LED~ ; access diagnostic LEDs
4000-4FFF RD or WR BOARD_C~ ; enable Board C functions:
4000-40FF RD or WR CS_MUX~ ; enable analog Mux to write
; enable 1st Bilevel latch to read
4100-41FF ; not used
4200-42FF CS_CONTROL1~ ; enable DCE-C Latch 1
4300-43FF CS_CONTROL2~ ; enable DCE-C Latch 2
4400-44FF RD or WR CS_DAC~ ; enable HV-setting DAC
4500-45FF RD only CS_BILEVEL~ ; enable 2nd Bilevel latch to read
4600-46FF RD only RD_LED~ ; read diagnostic LEDs CONFLICT
4700-47FF RD or WR CS_ADC~ ; access HK ADC

5000-5FFF RD or WR the interface registers (Actel internal), see next page

6000-7FFF RD or WR BOARD_A~ ; enable Board A Counter functions:

6000-60FF RD only CS_CNT_A~ ; access Counter A
6100-61FF RD only CS_CNT_B~ ; access Counter B
6200-62FF RD or WR CS_PHA_A~ ; access PHA A
6300-63FF RD or WR CS_PHA_B~ ; access PHA B

4000-4FFF RD or WR BUSIO~ ; enables DATA bus on Board B

6000-7FFF ; to communicate to Board A or C

DATA SPACE (PSEN = 1)

5000-5FFF RD or WR data BOARD_C ; enable these DCE-B Actel internal
; Command and HK functions:

50 RD only ; LSD of #0 Command Shift Register
; and GOT_IT clears BUSY w/o delay

51 ; next byte of #0

52 ; next byte of #0

53 ; MSD of #0 Command Shift Register

54 RD only ; LSD of #1 Command Shift Register

; and GOT_IT clears BUSY w/o delay

55 ; next byte of #1

56 ; next byte of #1

57 ; MSD of #1 Command Shift Register

50 WR only ; LSD of HouseKeeping Shift Register

51 ; next byte of HK

52 ; next byte of HK

53 ; MSD of HouseKeeping Shift Register

; and start shifting out w/o delay

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Here's a listing of the analog and bilevel channels
from the DCE-C housekeeping board:

40-channel HouseKeeping mux and fast 8-bit ADC

the analog muxes (HI-508's) are addressed and channels selected
with the following 8-bit addressing scheme (same as FUSE):

D0 = mux addressing bit A0

D1 = A1

D2 = A2

D3 = select MUX 1

D4 = select MUX 2

D5 = select MUX 3

D6 = select MUX 4

D7 = select MUX 5

the write address is CS_MUX~

to read one HouseKeeping input channel:

(1) set the desired MUX and mux channel (see next section)

the write address is CS_MUX~

(2) write to address CS_ADC~

(3) wait 2 usec or more

(4) read from address CS_ADC~

MUX 1 channels (0000 1xxx):

000 Detector 1 temperature

001 Door temperature

010 Filter Module temperature

011 HV temperature

100 TDC-A_X temperature

101 Ion Pump temperature 8 June 99

110 Amp-A temperature

111 Amp-B temperature

MUX 2 channels (0001 0xxx):

000 TDC-B_X temperature

001 Detector 2 temperature 8 June 99

010 LVPS temperature
011 DCE-B temperature
100 FStatus
101 +5V/1.25 = 4V
110 +15V/3.75 = 4V
111 -15V/-3.75 = 4V
MUX 3 channels (0010 0xxx):
000 Door Position
001 LVPS Aux_Mon
010 HV Imon A
011 HV Imon B
100 HV A monitor
101 HV B monitor
110 QStatus A
111 QStatus B
MUX 4 channels (0100 0xxx):
000 Aux Status
001 Motor Status
010 Actuator Status
011 LVPS PMon
100 HV-A programming voltage
101 HV-B programming voltage
110 TDC-A_X_Ana
111 TDC-A_Y_Ana
MUX 5 channels (1000 0xxx):
000 +5V_Mon from DCE-A
001 +5V_Mon from DCE-B
010 TDC-B_X_Ana
011 TDC-B_Y_Ana
100 HV-Max-A programming voltage 8 June 99
101 HV-Max-B programming voltage "
110 gnd 2 July 99
111 gnd "

read 8 bits for: D0 = Door Latched
D1 = Door Open
D2 = Door Closed
D3 = HV_ON
D4 = HV_ENA_1 status (to HVPS, at Safe Plug) 2 July 99
D5 = HV_ENA_2 status (to HV Filter Module, at Safe Plug)
D6 = HV_Enabled (Safe Plug is in)
D7 = Det_ID_0
the read address is CS_MUX~

read 8 bits for: D0 = Door Latched added 2 July 1999
D1 = Aux Power ENA
D2 = Actuator ENA
D3 = Motor ENA
D4 = Aux Power ON
D5 = HV0 status
D6 = Door_Enabled (Safe Plug is in)
D7 = Det_ID_1
the read address is CS_Bilevel~