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SUBJECT TITLE

DCE Hardware/Software Interface

KEYWORDS: COS, DCE, Control Segment

PREPARED BY	DATE	APPROVED BY	DATE
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SCOPE/TEXT: (ATTACH ADDITIONAL SHEETS AS REQUIRED)

This SER provides a description of the hardware/software interface for the COS Detector Control Electronics (DCE). This document describes all of the registers and I/O ports the DCE Flight Software uses to manipulate the detector hardware.

DISTRIBUTION:

see attached list

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1. Introduction

This SER defines the DCE software to hardware interfaces.

1.1 SER Overview

This SER contains the following sections:

- 1) Introduction

  This section provides an overview of the contents of this SER and of the DCE processor interfaces.

- 2) Control Segment Processor Memory Map

  This section provides a detailed description of the COS DCE processor interfaces.

1.2 References

[1] COS Memory Map Tables for the CS Electronics (SER COS-SW-tbd)

[2] COS DCE Flight Software Design Document (COS-UCB-009)

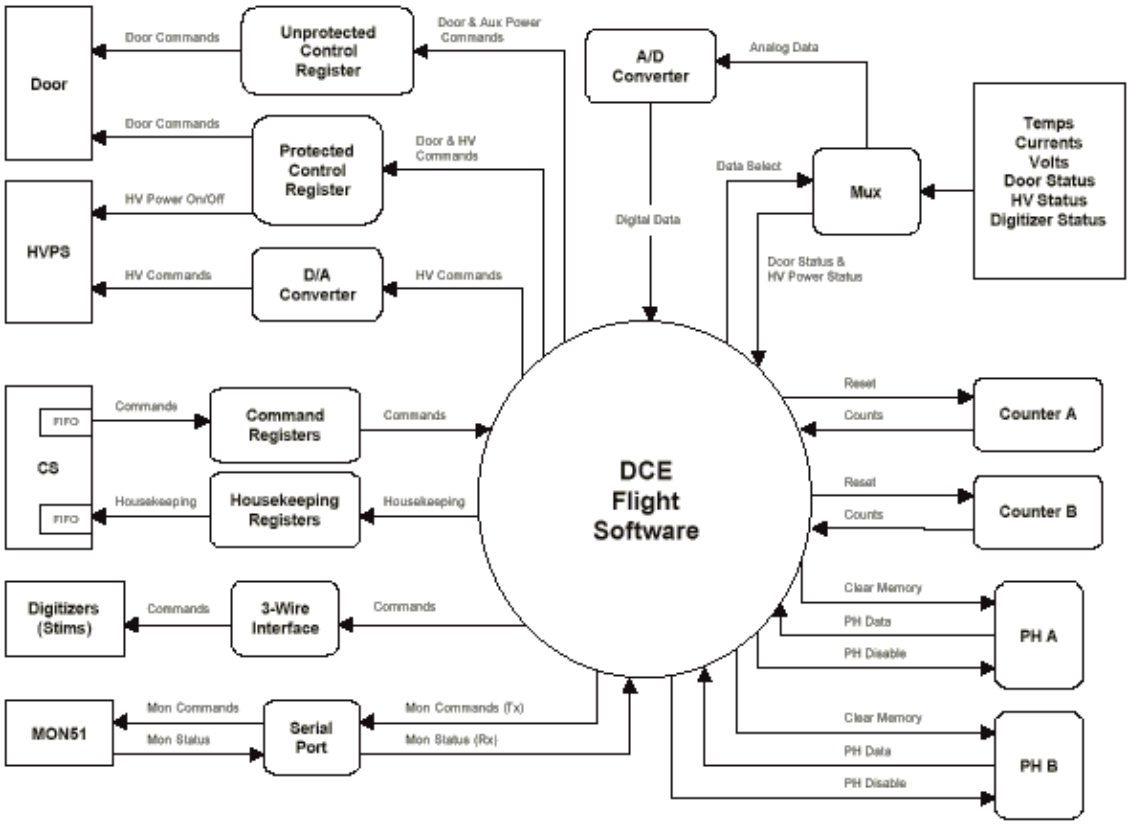


Figure 1. DCE Context Level Data Flow Diagram

Figure 1 shows the hardware to software interfaces as round corner boxes. This document describes each of these interfaces in detail.

2. Memory map, read and write registers and internal 8051 ports

This section gives the overall memory map, the memory mapped read registers, with the bitwise format of each, the write registers and the internal 8051 ports.

2.1 DCE Processor Memory Map

Interface	Address Low	Address High	Description	Legal Access Size - Bits
Low 8K RAM	0	3FFF	RAM Data and Code	8
Upload buffer	?	?	Stores upload data in this 1K block	8
Download Buffer	?	?	Stores download data in this 1K block	8
Housekeeping Buffer	?	?		
High 32K RAM				
Lower code area	8800	BFFF		8
Upper Code Area	C800	FFFF		8
Variables	8000	87FF		8
Memory - PROM	0	7FFF	ROM Code PROM on	32,16,8
Memory - PROM	0	3FFF	ROM Code	32,16,8

2.2 Memory Mapped Read Registers

Hardware Component	Address Range	Register Read Function	Register Size
Counter A	6000 - 60FF	Counter A value	16
Counter B	6100 - 61FF	Counter B value	16
PH A	6200 – 62FF	PH A value	16
PH B	6300 – 63FF	PH B value	16
Switches for Door, HV	4000 – 40FF	Reads door status(end switches and latch)	8
Control 1 Register	4200-42FF	Readback of unprotected control 1 register	8
Control 2 Register	4300-43FF	Readback of protected control 2 register	8
ADC Digitized temps/volts	4700 - 47FF	Digital voltage and temperature readings	16
Rx register	5000 - 5300	Registers for command traffic 3wire read	16

2.2.1 Counter A and B

Counters reflect the number of photon events that have passed through the various stages of the digitizing process. The FUV hardware has three types of counters: front end counters (FECA & FECB), digitized event counters (DECA & DECB), and science data counters (SDC1 & SDC2).

Register:
Address Range: 06000 to 060FF for counter A
06100 to 061FF for counter B

In this format:

Bit 0-15 => Counter Status – need specific format of data, and what it means.

2.2.2 PH A STATUS

Register:
Address Range: 06200 to 0623F for slice 0
06240 to 0627F for slice 1
06280 to 062BF for slice 2
062C0 to 062FF for slice 3

In this format:

Bit 0-15 => PH A Status – need specific format of data, and what it means.

2.2.3 PH B STATUS

Register:
Address Range: 06300 to 0633F for slice 0
06340 to 0637F for slice 1
06380 to 063BF for slice 2
063C0 to 063FF for slice 3

In this format:

Bit 0-15 => PH B Status – need specific format of data, and what it means.

2.2.4 Door Status

Register:
Address Range: 04000 to 040FF

In this format:

Bit 0-7 => Door Status – need specific format of data, and what it means.

2.2.5 ADC Digitized Temps/Volts

An analog-to-digital converter (ADC) converts sensor voltages to digital values that are stored in the housekeeping data area. The sensors can collect temperature, voltage or current information among other things. The FSW must use the multiplexer (MUX) to select the appropriate ADC input source. After selecting the desired source, the FSW must wait a short time for the input to settle. After waiting the settle time, the FSW reads the ADC converted value and stores it in the appropriate housekeeping location.

Here's a listing of the analog and bilevel channels
from the DCE-C housekeeping board:

40-channel HouseKeeping mux and fast 8-bit ADC
the analog muxes (HI-508's) are addressed and channels selected
with the following 8-bit addressing scheme (same as FUSE):
D0 = mux addressing bit A0
D1 = A1
D2 = A2
D3 = select MUX 1
D4 = select MUX 2
D5 = select MUX 3
D6 = select MUX 4
D7 = select MUX 5
the write address is CS_MUX~
to read one HouseKeeping input channel:
(1) set the desired MUX and mux channel (see next section)
the write address is CS_MUX~
(2) write to address CS_ADC~
(3) wait 2 usec or more
(4) read from address CS_ADC~

MUX 1 channels (0000 1xxx):
000 Detector 1 temperature
001 Door temperature
010 Filter Module temperature
011 HV temperature
100 TDC-A_X temperature
101 Ion Pump temperature 8 June 99
110 Amp-A temperature
111 Amp-B temperature

MUX 2 channels (0001 0xxx):
000 TDC-B_X temperature
001 Detector 2 temperature 8 June 99
010 LVPS temperature
011 DCE-B temperature
100 FStatus
101 +5V/1.25 = 4V
110 +15V/3.75 = 4V
111 -15V/-3.75 = 4V

MUX 3 channels (0010 0xxx):

000 Door Position
001 LVPS Aux_Mon
010 HV Imon A
011 HV Imon B
100 HV A monitor
101 HV B monitor
110 QStatus A
111 QStatus B

MUX 4 channels (0100 0xxx):
000 Aux Status
001 Motor Status
010 Actuator Status
011 LVPS PMon
100 HV-A programming voltage
101 HV-B programming voltage
110 TDC-A_X_Ana
111 TDC-A_Y_Ana

MUX 5 channels (1000 0xxx):
000 +5V_Mon from DCE-A
001 +5V_Mon from DCE-B
010 TDC-B_X_Ana
011 TDC-B_Y_Ana
100 HV-Max-A programming voltage
101 HV-Max-B programming voltage "
110 gnd
111 gnd "

read 8 bits for: D0 = Door Latched
D1 = Door Open
D2 = Door Closed
D3 = HV_ON
D4 = HV_ENA_1 status (to HVPS, at Safe Plug)
D5 = HV_ENA_2 status (to HV Filter Module, at Safe Plug)
D6 = HV_Enabled (Safe Plug is in)
D7 = Det_ID_0
the read address is CS_MUX~

read 8 bits for: D0 = Door Latched
D1 = Aux Power ENA
D2 = Actuator ENA
D3 = Motor ENA
D4 = Aux Power ON
D5 = HV0 status
D6 = Door_Enabled (Safe Plug is in)
D7 = Det_ID_1
the read address is CS_Bilevel~

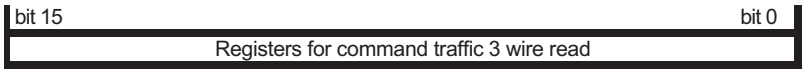
Register:
Address Range: 04700 to 047FF

In this format:

Bit 0-15 => ADC Digitized Temps/Volts – need specific format of data, and how it is read.

2.2.6 Rx register

Register:
Address Range: 05000 to 05300



In this format:

Bit 0-15 => Rx Register – need specific format of data, and what it means.

2.3 Memory Mapped Write Registers

Hardware Component	Address Range	Register Write Function	Register Size
HV DAC A Setting	4101	High voltage commands to detector head segment A	8
HV DAC B Setting	4103	High voltage commands to detector head segment B	8
HV DAC A Max	4100	High voltage commands to detector head segment A	8
HV DAC B Max	4102	High voltage commands to detector head segment B	8
Control Bits for door, Aux power	4200 - 42FF	Unprotected Control Register	8
Control Bits for door, HV	4200 - 42FF	Protected Control Register	8
MUX select input to ADC	4000 – 40FF	MUX Data select	8
ADC	4700 – 47FF	ADC start	8
Tx registers for housekeeping traffic	5000 - 5300	3 wire write	8
LEDs	2000 – 3FFF	Not used for flight	8

The DCE FSW controls the high-voltage power supply (HVPS) and the door mechanism by setting and clearing bits in one of two control registers. The control bits that can cause severe degradation to the FUV detector if used incorrectly are allocated to a protected control register that has been equipped with a *lock* bit. The remaining control bits that cannot cause damage to the FUV detector have been allocated to an unprotected control register.

2.3.1 Protected Control Register

The control bits allocated to this register are as follows:

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Lock	NU	Door On	Act A and B	Door Override	PROM Enable	HV Enable	Ion pump

Bit 0 *Ion pump on/off* => - for GSE use only since ion pumps are not used in orbit
Bit 1 *HV enable* => turns on/off power to both the grid & MCP
Bit 2 *PROM enable* => enables/disables the PROM
Bit 3 *Door end switch override*
Bit 4 *Actuator A and B on* =>turns on/off power to actuators A and B
Bit 5 *Door motor on* => turns on/off power to the door motor
Bit 6 *NU=> Not Used*
Bit 7 Lock Bit

2.3.2 Unprotected Control Register

The unprotected control register contains control bits that cannot damage the FUV detector. The control bits allocated to this register are as follows:

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
NU	NU	NU	NU	NU	Act Enable	Door Dir	Aux Pwr En

Bit 0 *Aux power enable* => enables auxiliary power for moving the door motor or actuators
Bit 1 *Door direction* => sets the direction of a door move
Bit 2 *Actuator enable* => enables the actuators
Bit 3 *NU=> Not Used*
Bit 4 *NU=> Not Used*
Bit 5 *NU=> Not Used*
Bit 6 *NU=> Not Used*
Bit 7 *NU=> Not Used*

2.3.3 HVPS Digital-to-Analog Converter (DAC)

The DCE FSW uses the High-Voltage Power Supply (HVPS) Digital-to-Analog Converter (DAC) to control the HVPS. The DAC converts a digital value to a high-voltage value in the 2000 to 6000 volt range at the detector head. The exact conversion coefficients for the DAC-to-HV relationship are specified in the list of housekeeping items. The DCE FSW uses the DAC to command the HVPS to a new voltage level. Status information concerning the state of the HVPS is returned to the FSW via the multiplexer (MUX) and Analog-to-Digital Converter (ADC). The multiplexer is used to select the appropriate input to the analog-to-digital converter. There are a number of possible ADC inputs that can be selected using the MUX.

4100 HV Cmds to detector segment A

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HV DAC A Max							

4101 HV Cmds to detector segment A

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HV DAC A Setting							

4102 HV Cmds to detector segment B

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HV DAC B Max							

4103 HV Cmds to detector segment B

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HV DAC B Setting							

2.4 Internal 8051 Registers

Ports are 8-bit latches that provide hardware control similar to memory mapped I/O (e.g. flipping a bit in a hardware latch). They are not, however, addressed using external memory addresses. They are accessed internal to the 8051 using a series of 256 registers. Each register has a unique address (0-255). The ports are mapped to internal 8051 address space. To access a port (or port register), special 8051 instructions are used to access a port's memory location (read/write). These instructions are different than those used to access MMIO.
The software can access individual bits by using a bit address, rather than a port address. The bit address can be used to toggle individual bits in the various port registers whereas port registers access 8-bit values. The bit addresses essentially overlay the port registers. Only a certain range of port registers can be accessed using bit addresses. The bit addresses are also set/cleared using a special 8051 machine language instruction that is different from the port register access instructions.
Figure 4.3-1 provides an overview of how ports are mapped to internal 8051 memory. It shows how accessing different internal memory ranges provides different types of access to the ports. The MCS 51 Micro-controller Family User's Manual should be consulted for specific information about 8051 ports.

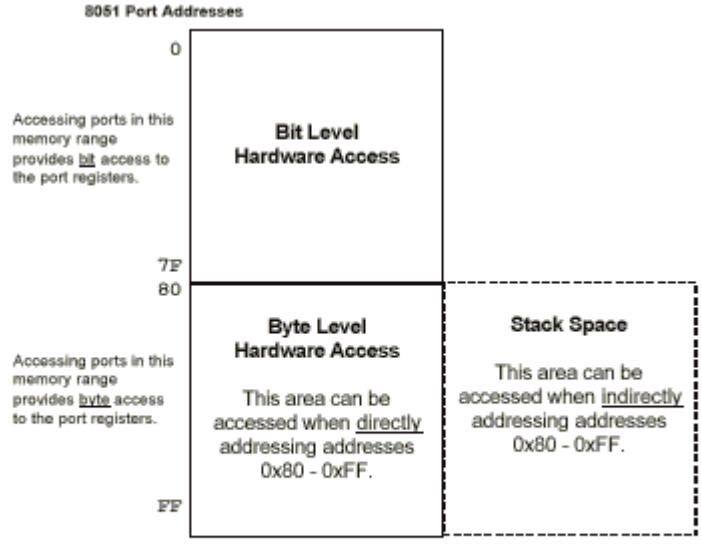


Figure 4.3-1. Port Mapping of Internal 8051 Memory

The following is a list of DCE hardware that is controlled using ports:
· *Digitizer 3-Wire Interface*

- *Lock Bit*
- *B0/B1 Memory Select Bits*
- *Pulse Height Memory Disable Bit*
- *Serial I/O Port*
- *Self-Reset Bit*
- *Timer*
- *Interrupt*

2.4.1 Digitizer 3-Wire Interface

The digitizer is the electronics that interprets photon events. The criterion used to qualify an event can be controlled via commands. The digitizers commands are sent via a synchronous serial link implemented with 8051 port pins. The digitizer returns setting talkbacks as an input to the MUX/ADC. The digitizer is programmed with default values upon power-on reset, and after that, settings are modified only on command.

The DCE FSW uses a 3-wire interface to send commands to the digitizer hardware.

1) Physical interface: There are three signals which go from the DCE to the Digitizer Y board (assuming there is a separate 3 wire interface to the A and B segments(???)). These signals have the names BSTB, BCLK, and BCMD at the interface to the Y Actel in the current schematic. BSTB is essentially an enable (enable=1), BCLK is a software generated clock (not necessarily a symmetrical clock) that is high for 1.5 microseconds. BCMD is the serial data values (16 bits in all). Data is latched on the rising edge.
2) Word structure: The Data is a sixteen bit word sent MSb first. The structure is as follows

   Msb Lsb
   0xxx 0yyy zzzzzzzz
   Where “xxx” is the “chip select” for the DACs and Mux’s, “yyy” is the address for the chip selected, and “zzzzzzzz” is the data value to be latched to the DAC (Non-applicable for the Mux).
3) the Y Actel will clock in the 16 bits of data and, on the falling edge of BSTB, that data will be latched. On the next clock cycle (4MHz clk), the data will be presented to the DAC’s and Mux’s accordingly.
4) There are 3 DACs and 3 Mux’s. The Most Significant Nibble (MSN) will select chips according to the following table:

Bit # 14*	Bit # 13	Bit # 12	selected
0	0	0	DAC0
0	0	1	DAC1
0	1	0	DAC2
0	1	1	UNDEFINED
1	0	0	MUX0
1	0	1	MUX1
1	1	0	MUX2
1	1	1	STIM ACTIVE

*note: Bit 15 will be ignored, it could be used to validate a command by demanding that it be zero—this decision can be made prior to the flight chip being burned.

5) DAC#0 handles settings for the X digitizer, DAC#1 handles timing and charge thresholds, and DAC#2 handles settings for the Y digitizer. The “yyy” values select the following values depending on the values of “xxx”

Bit 10*	Bit 9	Bit 8	DAC#0	DAC#1	DAC#2	MUX0	MUX1	MUX2
0	0	0	X_SHIFT	TTHR_Y	Y_SHIFT -	X_SHIFT	+15	Y_SHIFT
0	0	1	X_STRETCH	Q_LO	Y_STRETCH	X_STRETCH	-15	Y_STRETCH
0	1	0	B_WALK_X	Q_HI	B_WALK_Y	B_WALK_X	Vcc	B_WALK_Y
0	1	1	E_WALK_X	TTHR_X	E_WALK_Y	E_WALK_X	-5.2	E_WALK_Y
1	0	0	-	-	-	TTHR_Y	VREF	GND
1	0	1	-	-	-	Q_LO	GND	GND
1	1	0	-	-	-	Q_HI	GND	GND
1	1	1	-	-	-	TTHR_X	GND	GND

*note: Bit 11 will be ignored, it could be used to validate a command by demanding that it be zero—this decision can be made prior to the flight chip being burned.

6) Although it doesn't really matter from the Actel design point of view, I will assume that operationally, you first send a command to set a particular DAC value, then issue another command to output that value on the Mux. Once the DAC is set, it remains set, only one mux value can be selected at a time. (????)

2.4.2 Lock Bit

Locks and unlocks the protected control register.

2.4.3 B0/B1 Memory Select Bits

External memory bank select. Effectively allows memory ranges to be re-mapped. This means that by configuring the bits a certain way, you can change "code" address space from PROM to RAM without changing the executable image.

2.4.4 Pulse Height Memory Disable Bit

Disables access to the PH memory by the science data (PH) processing hardware. This is done while the PH memory is being accessed by the 8051 to avoid both the 8051 and PH hardware from accessing the PH memory at the same time.

2.4.5 Serial I/O Port

The serial I/O port is a feature built-in to the 8051 microcontroller. It is used to provide a back door method of communicating with the DCE FSW. Test versions of the DCE FSW might include capabilities to use the serial I/O port for communicating with special COTS test software (MON51). Special inspect-and-change software that uses the serial port to communicate with the MON51 software would only be included in test versions of the DCE FSW.

2.4.6 Pulse Height Histograms

Pulse Height (PH) Histogram data consists of 128 bins of consecutive 16-bit words. The PH Counter hardware design requires the 8051 to assert a PH disable signal while accessing the PH Counter memory and de-assert the signal when done.

2.4.7 Self-Reset Bit

Allows the DCE flight software to reset itself.

2.4.8 Timer

The 8051 has 3 internal timers (0, 1 and 2). Timers 0 and 1 are used in series to provide the timer tick.

2.4.9 Interrupt Controller

The 8051 has an internal interrupt controller with 8 hard-wired interrupts.

2.5 CS to Command/Houskeeping Interface

Control Section to Detector Interface Registers

Address Range	Register Size	Register Read Function	Register Write Function	Register Access Function
06500000	32 Bits	Null Content	FUV command register	N/A
06500008	32 Bits	spare telemetry register	spare command register	N/A
0650000C	32 Bits	Null Content	FUV discrete control register	N/A
06500014	4 Bits	spare discrete status register	spare discrete control register	N/A

0650 0000: FUV Command Register: Writing to this register causes the data written to be shifted serially, most significant bit first, to the FUV detector command receive port. Reading from this register returns all zeros.

Operation	BIT 31(MSB), BIT 30, BIT29, ... BIT 0(LSB)
READ	0000 0000
WRITE	FUV command word

0650 000C: FUV Discrete Register: When writing to this register, bit 3 controls the reset signal to the DCE. Bit 3 must be set to a '1' to engage the reset operation. The default state for this register is 0000 0000h. Any values written to this register will remain until changed by additional write operations, with the exception of a CS reset which will set this register to it's default state. Reading from this register returns the status of the busy condition in bit 0. If bit 0 = 1, the DCE cannot accept another command.

Operation	BIT 31 .... BIT 4	bit 3	bit 2	bit 1	bit 0
READ	0000 000	0	0	0	busy bit: 1=busy, 0 = NOT busy
WRITE	XXXX XXX	reset bit: 1 = reset, 0 = no effect	X	X	X

2.5.1 DCE Housekeeping Interface

DCE housekeeping data is transmitted serially from the DCE to the MEB. The 32 bit gated serial data is converted to parallel data and written into a FIFO. FIFO data and FIFO flags are available to the CS via memory mapped IO. The FIFO is 4096 32-bit words deep. An interrupt to the CS is generated when the FIFO is not empty. It is possible to use the fast MOVS assembly instruction when reading from this FIFO. Since the FIFO is 4096 deep and 4 bytes wide, 16 Kbytes of memory space are allocated for the FIFO address. Although 16 Kbytes of address space accesses the FIFO, all accesses must be on 32 bit boundaries and regardless of the address, data is retrieved in a First In First Out fashion. Table 2.5.1 displays the address map for the DCE housekeeping interface.

Table 2.5.1

CS ADDRESS (hex)	COMM Read Function	COMM Write Function
0650 00A0	Null Content	RESET Housekeeping FIFOs
0650 00A4	DCE Housekeeping FIFO flags	No Effect
0654 4000 – 0654 7FFE	DCE Housekeeping Data	No Effect

0650 00A0: Reset Housekeeping FIFOs: Writing to this memory location causes the Housekeeping FIFOs to reset. The data written has no effect. A read operation returns all zeros.

Operation	BIT 31(MSB) ... BIT 0(LSB)
READ	0000 0000
WRITE	XXXX XXXX

0650 000C: Housekeeping FIFO flags: Writing to this register has no effect. Reading from this register returns the Housekeeping FIFOs flags. The flags are active LOW, i.e. if the Empty Flag (bit 0) = '0' then the FIFO is empty.

Operation	BIT 31 .... BIT 4	bit 3	bit 2	bit 1	bit 0
READ	0000 000	0	Full%	Half Full%	Empty%
WRITE	XXXX XXX	X	X	X	X

0654 4000 – 0650 7FFE: Housekeeping Data: Writing to these memory locations has no effect. Reading from these locations returns the Housekeeping data.

Operation	BIT 31(MSB) ... BIT 0(LSB)
READ	Housekeeping Data
WRITE	XXXX XXXX

Notes to be included:

Here's some text listings of the various addresses
and chip-selects within the COS DCE:

This is the address decoding scheme for the COS DCE-B Actel-CPU. Rev A
CODE SPACE (PSEN = 0 and PROM ON)
0000-7FFF PSEN code only CS_ROM~ ; read code from non-flight EPROM
0000-1FFF PSEN code only CS_ROM0~ ; read PROM 0
2000-3FFF PSEN code only CS_ROM1~ ; read PROM 1

(PSEN = don't care)
0000-FFFF RD or data or RD_RAM~ ; access Static RAM
PSEN code ; (write to SRAM using WR*)
new: 0000-3FFF RD or WR code CS_LowRAM~ ; 16k of extra data SRAM
(PROM OFF) ; for interrupt tables
8000-FFFF data or code CS_RAM~ ; access RAM (high)

DATA SPACE (PSEN = 1)
new: 0000-3FFF RD or WR CS_LowRAM~ ; 16k of extra data SRAM
(PROM ON)
2000-2FFF WR CS_LED~ ; access diagnostic LEDs
4000-4FFF RD or WR BOARD_C~ ; enable Board C functions:
4000-40FF RD or WR CS_MUX~ ; enable analog Mux to write
; enable 1st Bilevel latch to read
4100-41FF ; not used
4200-42FF CS_CONTROL1~ ; enable DCE-C Latch 1
4300-43FF CS_CONTROL2~ ; enable DCE-C Latch 2
4400-44FF RD or WR CS_DAC~ ; enable HV-setting DAC
4500-45FF RD only CS_BILEVEL~ ; enable 2nd Bilevel latch to read
4600-46FF RD only RD_LED~ ; read diagnostic LEDs CONFLICT
4700-47FF RD or WR CS_ADC~ ; access HK ADC

5000-5FFF RD or WR the interface registers (Actel internal), see next page

6000-7FFF RD or WR BOARD_A~ ; enable Board A Counter functions:
6000-60FF RD only CS_CNT_A~ ; access Counter A
6100-61FF RD only CS_CNT_B~ ; access Counter B
6200-62FF RD or WR CS_PHA_A~ ; access PHA A
6300-63FF RD or WR CS_PHA_B~ ; access PHA B

4000-4FFF RD or WR BUSIO~ ; enables DATA bus on Board B
6000-7FFF ; to communicate to Board A or C
DATA SPACE (PSEN = 1)
5000-5FFF RD or WR data BOARDC ; enable these DCE-B Actel internal
; Command and HK functions:
50 RD only ; LSD of #0 Command Shift Register
; and GOT_IT clears BUSY w/o delay
51 ; next byte of #0
52 ; next byte of #0
53 ; MSD of #0 Command Shift Register

54 RD only ; LSD of #1 Command Shift Register
; and GOT_IT clears BUSY w/o delay
55 ; next byte of #1
56 ; next byte of #1
57 ; MSD of #1 Command Shift Register

50 WR only ; LSD of HouseKeeping Shift Register
51 ; next byte of HK
52 ; next byte of HK
53 ; MSD of HouseKeeping Shift Register
; and start shifting out w/o delay