Technical Evaluation Report

"DCE BOOT/OPERATE Interface Specification"

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Prepared By:	Dr. William Clement	8-28-00
	Dr. William Clement, COS Software Consultant	Date
Reviewed By:	Daniel Blackman	
	Daniel Blackman, DCE Software Integration	Date
Reviewed By:	Geoff Gaines	9-1-00
	Geoff Gaines, FUV Detector Systems Engineer	Date
Approved By:	Dr. Kenneth Brownsberger	8-25-00
	Dr. Kenneth Brownsberger, COS Instrument Scientist	Date
Approved By:	Barry Welsh	8-31-00
	Barry Welsh, FUV Detector Program Manager	Date
Approved By:	John Andrews	8-24-00
	John Andrews, COS Experiment Manager	Date

Center for Astrophysics & Space Astronomy
University of Colorado
Campus Box 593
Boulder, Colorado 80309

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1. BOOT-TO-OPERATE INTERFACE SPECIFICATION

In order to facilitate the parallel development of the two COS DCE software packages, BOOT and OPERATE, the following interface requirements apply.

1.1 INTERRUPT LOCATIONS

One bit of 8051 bit-addressable memory defines the destination of interrupt calls. Naming this bit "IVEC", the following actions follow:

- IVEC = 0: ISRs are located in PROM for BOOT mode. Flight software jumps directly to the appropriate ISR. This is normal 8051 behavior.

- IVEC = 1: ISRs are located in RAM for OPERATE mode purposes. Upon receipt of an interrupt, the code in PROM (BOOT code) forces a jump to an address 8000h bytes above the hardware interrupt vector. It is presumed that the OPERATE mode software will locate actual interrupt vectors at these locations, causing another jump to the actual OPERATE mode ISR.

Interrupt Source	BOOT Mode Interrupt Vector location (IVEC=0)	OPERATE Mode Interrupt Vector location (IVEC=1)
External 0	0003h	8003h
Timer 0	000Bh	800Bh
External 1	0013h	8013h
Timer 1	001Bh	801Bh
Serial Port	0023h	8023h
Timer 2	002Bh	802Bh
PCA Timer	0033h	8033h

- IVEC will be located at the last bit-addressable location in 8051 internal memory (Address: 2F.7h). BOOT and OPERATE modes must protect this bit.

- BOOT and OPERATE are each responsible for setting IVEC to the appropriate value in their own initialization sequences, i.e., during BOOT mode initialization, BOOT must set IVEC = 0. During OPERATE mode initialization, OPERATE must set IVEC = 1.

1.2 OPERATE ENTRY POINT

Entry to OPERATE mode from BOOT for the "Jump to OPERATE" command will cause BOOT to jump to address 8000h. OPERATE mode must ensure that addresses 8000h – 8002h contain a jump to the actual entry/reentry point in the OPERATE mode software.

1.3 MEMORY MANAGEMENT

BOOT mode will not initialize any memory for OPERATE mode. BOOT and OPERATE are each responsible for initializing memory for their own purposes. BOOT shall not overwrite nor initialize the OPERATE mode areas – as defined in Section 2 (DCE Memory Map). OPERATE shall not overwrite nor initialize the BOOT mode areas – as specified in Section 2 (DCE Memory Map). The only common data items that BOOT and OPERATE both manage are the IVEC bit – as specified in Section 1.1 (Interrupt Locations), and the Reset Memory Pattern area – as specified in Section 1.4 (Reset-Type Indication).

1.4 RESET-TYPE INDICATION

A 6-Byte Reset Memory Pattern of: 55h AAh 00h FFh 9Bh 64h (little-endian format) (Binary: 01010101 10101010 00000000 11111111 10011011 01100100) at address 3FFAh is used by BOOT mode to determine if a DCE Reset is a Power-ON Reset or a Watchdog Reset. If the 6-Bytes starting at 3FFAh matches the Reset Memory Pattern – then BOOT mode will assume the DCE Reset is a Watchdog Reset. Otherwise, BOOT mode will assume the DCE Reset is a Power-ON Reset. During the Reset Initialization sequence, BOOT mode will write the Reset Memory Pattern to address 3FFAh. Consequently, both BOOT and OPERATE modes must scramble this memory pattern when executing the Power-ON Reset Command (LFDRSTP).

2. DCE MEMORY MAP

Address (Start of Segment)	CODE Space	External Data Space
0000h	BOOT Mode Reset Vector	
0003h	BOOT External 0 Interrupt Vector	
000Bh	BOOT Timer 0 Interrupt Vector	
0013h	BOOT External 1 Interrupt Vector	
001Bh	BOOT Timer 1 Interrupt Vector	
0023h	BOOT Serial Port Interrupt Vector	
002Bh	BOOT Timer 2 Interrupt Vector	
0033h	BOOT PCA Timer Interrupt Vector	
0040h	BOOT Code	OPERATE Mode Upload Data
0440h		OPERATE Mode Command Packet
045Ch		unused
1040h		OPERATE Mode Download Data
1440h		OPERATE Mode Housekeeping Packet
1840h		unused
2040h		BOOT Mode Upload Data
2440h		BOOT Mode Command Packet
245Ch		BOOT Mode Patchable Constants
3040h		BOOT Mode Download Data
3440h		BOOT Mode Housekeeping Packet
3840h		unused
3FFAh		**Reset Memory Pattern**
4000H	Not physically present	Memory Mapped I/O
8000h	OPERATE Mode Entry Vector	
8003h	OPERATE External 0 Interrupt Vector	
800Bh	OPERATE Timer 0 Interrupt Vector	
8013h	OPERATE External 1 Interrupt Vector	
801Bh	OPERATE Timer 1 Interrupt Vector	
8023h	OPERATE Serial Port Interrupt Vector	
802Bh	OPERATE Timer 2 Interrupt Vector	
8033h	OPERATE PCA Timer Interrupt Vector	
8040h	OPERATE Code, Patchable Constants and Data	
FFFFh	end of memory	