COS DCE BOOT FSW v1.09 Component Test Results
Requirement 5.1.1.5c Code in PROM

Date:	February 13, 2001
Document Number:	COS-03-0015
Revision:	Initial Release
Contract No.:	NAS5-98043
CDRL No.:	N/A

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Letter	ECO No.	Description	Check	Approved	Date
-		Initial Release			

Original Release Name	Date
Drawn: K. Brownsberger	2-13-01
Reviewed:	
Approved:	

THE UNIVERSITY OF COLORADO
At Boulder
The Center for Astrophysics and Space Astronomy

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Size	Code Indent No.	Document No.	Rev
A		COS-03-0015	-
Scale: N/A			

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1. INTRODUCTION

1.1 PURPOSE

This document presents the Cosmic Origins Spectrograph (COS) Device Control Electronics (DCE) Flight Software (FSW) certification procedure. The purpose of this procedure is to verify that the FSW satisfies Software Requirements according to the method specified in the DCE FSW Test Plan (STP).

1.2 SCOPE

This test procedure comprises the steps necessary to verify that the FSW satisfies Software Requirements Document (SRD) paragraph 5.1.1.5 — Code in PROM: Verify that [Boot State code] transfers control to the Operate State code area.

1.3 LIMITATIONS AND CONSTRAINTS

This test cannot be run in parallel with any other commanding activity directed at the DCE FSW (such as, for example, the periodic transmission of NOOP commands). Test hardware shall be visually inspected, and its configuration noted, prior to conducting this test.

1.4 PROCEDURE OVERVIEW

The procedure requires the **hks** tools running on the Sun SparcStation Electronic Ground Support Equipment (EGSE) whose network IP address is one of

shorty.ssl.berkeley.edu
taiyo.ssl.berkeley.edu
ginger.ssl.berkeley.edu.

Test time shall be scheduled in advance. The Test Conductor must be logged into the Unix system as user **eagcos**, and be commanding from the appropriate directory. This directory contains both the test script file and the shell script file; these two files control test execution. The test is conducted by invoking the shell script. This shell script in turn invokes the Perl 5 program **UniScript.pl**, which resides in its own distinct directory. The test procedure steps have been pre-recorded in the test script file, and are executed interpretively by the **UniScript** program. The shell script and test script are attached to this document as appendices. As **UniScript** executes the test script it sends results to the operator console and to two report files, which are also placed in the current directory. After completion of the test script, the Test Conductor can certify successful test

execution by examining the contents of the report files and determining that required outputs are present in them. Printed copies of the report files are attached to the manually completed checklist (Paragraph 4 below) as documentation of the test.

1.5 THEORY OF TEST

The test relies on two quantifiable factors to verify that the FSW is in Operate State: first, that the **LFDOPERT** bit will be 1; second, that the transition from Boot State to Operate State resets the timer. The script forces Boot State by emitting a **POR** packet (0x80000000). It then assures a timer value of nine (9) seconds (or greater) by executing a nine-second **WAIT**. Following this interval the script issues an **LFDJMPCS** command, which should force Operate State. This is followed by a request for HK data, from which both **LFDOPERT** and **LFCTIME** can be determined. The former should be 1 and the latter should have a value (substantially) less than 9.

1.6 TEST SCRIPT IMPLEMENTATION

The test implements the operations described in Section 1.5 by means of standard **UniScript** directives and commands.

2. SPECIAL INSTRUCTIONS

2.1 QUALITY ASSURANCE

QA support is required to verify the configuration and setup environment as well as monitoring test steps and verifying results.

2.2 SAFETY

2.2.1 Personal Safety

To ensure the safety of the test personnel during test execution the guidelines contained in Paragraph 3.4, Reference [1] will be adhered to.

2.2.2 Test Article and Equipment Safety

- If access within one (1) meter of COS bench electronics is necessary, wrist straps attached to technical ground shall be used by all personnel involved in handling of any COS test article. Overcurrent and overvoltage shall be set to remove power if nominal limits are exceeded.

- Emergency Power Shutdown — If, during the COS DCE FSW test, power is ON and a severe test equipment failure results in the power system exceeding specified limits, the Test Conductor shall direct or perform shutdown of power.

2.3 CONTAMINATION

All flight hardware shall be handled with clean latex gloves; it shall be covered with clean ESD material and/or stored in a clean flow-bench.

3. SUPPORT REQUIREMENTS

3.1 PERSONNEL

Execution of the COS DCE FSW certification procedure requires the following personnel (to be completed at the Test Readiness Review (TRR):

Test Director: _____

Test Conductor: _____

Test Technician: _____

QA: _____

3.2 TOOLS, EQUIPMENT, AND MATERIALS

The following is a list of tools, equipment, or materials required in this test. Record manufacturer and model, metrology, or property numbers of equipment used, where appropriate. Record calibration due dates where appropriate.

Boot Mode ROM: schematic **27C256**

Engineering Ground Support Equipment (see paragraph 1.4). Indicate specific configuration:

EGSE			DCE		
taiyo	**shorty**	**ginger**	**ETU**	**DCE #1**	**DCE #2**
	X			X	

3.3 DATA/SOFTWARE

The following files must be present:

Table 3-1: Required Program and Data Files

EGSE (shorty) Directory	File	Description
\disks\galex\users\galex\tcs\uniscript	**UniScript.pl**	**UniScript** interpreter
\disks\galex\users\galex\tcs\uniscript\stp5_1_1_5c	**u**	Shell script for this procedure
Ditto	**stp5_1_1_5c.tst**	Test script for this procedure (Appendix B)

In addition, the **hks** tools must be active. Directions for activating **hks** are given in UCB-COS-DOC-1118 (Paragraph 3.4, Reference [4]).

3.4 REQUIRED DOCUMENTATION

Reference	Document Number	Title
1	NHB 1700.1(V1-A)	*NASA Basic Safety Manual*
2	COS-03-0015	*DCE FSW Test Procedure 5.1.1.5c* (this document)
3	UCB-COS-008	*COS FUV Detector Software Test Plan*
4	UCB-COS-DOC-1118	*COS EGSE Startup Procedure*

4. PROCEDURE/TASK STEPS

4.1 PRE-OPERATION ACTIVITIES

4.1.1 Make Sure that **hks** Tools Are Active

Follow the procedure given in Paragraph 3.4, Reference [4].

4.1.2 Make Sure that the Proper ROM Is Installed

Visually verify that the ROM under test is installed: if EEPROM, in U18: if PROM, in U2 and U7.

4.1.3 Log In to the EGSE

Step	QA	Operator Entry/System Response	Description
1		C:\tcs\us> **telnet shorty.ssl.berkely.edu**	Establish connection to shorty via Telnet client program
2		Login: **tcs** Password:	Using telnet window, login as user **tcs**

4.1.4 Set Current Directory

Step	QA	Operator Entry/System Response	Description
3		tcs@shorty% **cd ~galex/tcs** tcs@shorty% **pwd** /disks/galex/users/galex/tcs	Change current directory as shown

4.1.5 Slogin as eagcos

Step	QA	Operator Entry/System Response	Description
4		tcs@shorty% **slogin –l eagcos shorty.ssl.berkeley.edu** eagcos@shorty.ssl.berkeley.edu's password: ***(get from SSL personnel)*** Last login: Sat Oct 7 10:41:05 2000 from auntem.ssl.berke Sun Microsystems Inc. SunOS 5.8 Generic February 2000 You have mail. COS EGSE software version: devel	slogin as **eagcos**; get password from SSL personnel

4.1.6 Set Current Directory

Step	QA	Operator Entry/System Response	Description
5		eagcos:shorty% **cd /disks/galex/users/galex/tcs/uniscript/stp5_1_1_5c** eagcos:shorty% **pwd** /disks/galex/users/galex/tcs/uniscript/stp5_1_1_5c	Change current directory as shown

4.1.7 Ensure that Proper Files are Present

Step	QA	Operator Entry/System Response	Description
6		eagcos@shorty% **ls –l** Total 12 -rw-r--r-- 1 tcs eag 1398 Oct 8 18:03 stp5_1_1_5c.tst -rw-r--r-- 1 tcs eag 62 Oct 9 17:44 u eagcos@shorty% **more < u** #!/bin/sh perl ../UniScript.pl stp5_1_1_5c "0,0,0,0,0,0,0,0"	List files; the **.tst** file and the shell script **u** should be present

4.2 OPERATION EXECUTION

4.2.1 Establish Initial Test Conditions

Step	QA	Operator Entry/System Response	Description
7		eagcos:shorty% **set path=($path ~dbb/scripts/bin)**	Set path as shown to enable access to hks tools

4.2.2 Execute the Script

Step	QA	Operator Entry/System Response	Description
8		eagcos:shorty% **sh u** $pstring=0,0,0,0,0,0,0,0 Parameters are: Script File: stp5_1_1_5c #0: 0 #1: 0 #2: 0 #3: 0 #4: 0 #5: 0 #6: 0 #7: 0 Report file >/disks/galex/users/galex/tcs/uniscript/stp5_1_1_5c/stp5_1_1_5c.rp1 successfully opened. Report file	Shell to **u**. You should see the accompanying output as **UniScript** executes

		>/disks/galex/users/galex/tcs/uniscript/stp5_1_1_5c /stp5_1_1_5c.rp2 successfully opened. Script file /disks/galex/users/galex/tcs/uniscript/stp5_1_1_5c/s tp5_1_1_5c.tst successfully opened at level 0. "First 10-second wait ..." LFDRSTP "Second 10-second wait ..." "Test 5.1.1.5c Succeeded"	

4.3 POST-OPERATION ACTIVITIES

4.3.1 Copy Reports to PC Files and Print Them

Using an FTP client, copy the **u**, **stp5_1_1_5c.tst**, **stp5_1_1_5c.rp1**, and **stp5_1_1_5c.rp2** files to appropriate PC files. Include these files as Appendices A, B, C, and D with this completed form.

4.3.2 Complete The Test Procedure Form

Ensure that all blank fields in this report are completed correctly and submit the completed report to QA.

SUMMARY SHEET

OPERATION TITLE: _____ WOA# _____

TEST ARTICLES IDENTIFICATION (including serial and/or part numbers):

_____

TASKS/STEPS COMPLETED: _____

_____

LOCATION: _____

TEST STARTED: TEST TERMINATED

TIME: _____ Hr/Min TIME: _____ Hr/Min

DATE: _____ DATE: _____

LOGS USED: _____

ANOMALY REPORTS GENERATED: _____

_____

COMMENTS: _____

_____

_____

_____

_____

TEST CONDUCTOR: _____

Signature/Date

QA REPRESENTATIVE: _____

Signature/Date

Appendix A. hell Script u

```
#!/bin/sh
pkill noopy
perl ../UniScript.pl stp5_1_1_5c "0,0,0,0,0,0,0,0"
cosnoopy&
```

Appendix B. Test Script stp5_1_1_5c.tst

```
; ********************************************************
; * DCE FSW Requirement 5.1.1.5c -- Code in PROM          *
; * ---------------------------------------------------- *
; * Verify ... [that Boot State code] transfers control to  *
; * the lower code image.                                 *
; ********************************************************
;
SYM        NSEC=5
ECHO       2
;
;*********************************************
;* Make sure we are in Boot State -- issue POR *
;*********************************************
;
WAIT       1
DTG        3,"(0) Issuing POR"
WTO        "Issuing POR"
POR
WAIT       NSEC,HK
LOG        1,LFSBITS1,LFDOPERT
CHECK      1,(($LFSBITS1 & $LFDOPERT) == 0)
DTG        3,"DCE is in Boot State"
;
;*****************************************************
;* Jump to Code in External Memory. Verify this by    *
;* checking LFDOPERT and the timer LFCTIME            *
;* ------------------------------------------------- *
;* First, let LFCTIME build up by waiting 9 seconds   *
;* Then do the LFDJMPCS and, as quickly as possible,  *
;* check the new value of LFCTIME. It should be < 9!  *
;*****************************************************
;
; ********************************
; * Some tester entertainment ... *
; ********************************
;
DTG        3,"(1) Beginning 9-second wait..."
WTO        "Beginning 9-second wait..."
WTO        "9 seconds to go: >        |   "
WAIT       1
WTO        "8 seconds to go: ->       |   "
WAIT       1
WTO        "7 seconds to go: -->      |   "
WAIT       1
WTO        "6 seconds to go: --->     |   "
WAIT       1
WTO        "5 seconds to go:  --->    |   "
WAIT       1
WTO        "4 seconds to go:   --->   |   "
WAIT       1
WTO        "3 seconds to go:    --->  |   "
WAIT       1
WTO        "2 seconds to go:     ---> |   "
WAIT       1
WTO        "1 second  to go:      --->|   "
WAIT       1
WTO        "Ka-boom!!                ...  "
LOG        1,LFCTIME,LFDOPERT
;
LFDJMPCS   0
WAIT       10,HK
LOG        1,LFCTIME,LFDOPERT
CHECK      1,(($LFSBITS1 & $LFDOPERT) != 0)
CHECK      1,($LFCTIME < 9)
DTG        1,"(2) Test stp5_1_1_5c completed successfully"
WTO        "Test stp5_1_1_5c completed successfully"
```

Appendix C. Test Report stp5_1_1_5c.rp1

```
55555           1            1          55555
                                       5             11            11           5
                     ssss  ttttt  pppp   555            1             1           555
cccc
                    s        t    p   p     5            1             1              5
c
                    sssss    t    pppp       5          1             1               5
c
                        s    t    p      5   5          1             1           5   5
c
                    ssss     t    p       555   _____   111   _____   111   _____   555
cccc

Ver 17200  Thu Nov 16 19:20:25 2000    "(0) Issuing two PORs"

LFDNOOP

Addr Addr HK-Name         Value
---- ---- -------------- -----
16F4-16F5 LFSBITS1        0000

Addr Mask HK-Bit-Name     Value
---- ---- -------------- -----
16F4 0008 LFDOPERT        0

CHECK:   (($LFSBITS1 & $LFDOPERT) == 0)
eval:    ((0000 & 0008) == 0)

S U C C E S S

Ver 01.09  Thu Nov 16 19:20:30 2000    "(1) DCE is in Boot State"

Ver 01.09  Thu Nov 16 19:20:30 2000    "(2) Beginning 9-second wait..."

Addr Addr HK-Name         Value
---- ---- -------------- -----
1680-1683 LFCTIME         00000000

Addr Mask HK-Bit-Name     Value
---- ---- -------------- -----
16F4 0008 LFDOPERT        0

LFDJMPCS

Addr Addr HK-Name         Value
---- ---- -------------- -----
1680-1683 LFCTIME         00000002

Addr Mask HK-Bit-Name     Value
---- ---- -------------- -----
16F4 0008 LFDOPERT        1

CHECK:   (($LFSBITS1 & $LFDOPERT) != 0)
eval:    ((4008 & 0008) != 0)

S U C C E S S

CHECK:   ($LFCTIME < 9)
eval:    (0002 < 9)

S U C C E S S

Ver 17200  Thu Nov 16 19:20:44 2000    "(3) Test stp5_1_1_5c completed successfully"
```

Appendix D. Test Report stp5_1_1_5c.rp2

```
55555           1             1           55555
                                          5              11            11           5
                     ssss  ttttt  pppp   555             1             1           555
cccc
                    s        t    p   p     5            1             1              5
c
                    sssss    t    pppp       5           1             1               5
c
                        s    t    p      5   5           1             1           5   5
c
                    ssss     t    p       555   _____   111   _____   111   _____   555
cccc

Ver 17200  Thu Nov 16 19:20:25 2000    "(0) Issuing two PORs"

-------------------------------------------------------------------------
                         P O R   P A C K E T
-------------------------------------------------------------------------
80000000
-------------------------------------------------------------------------

-------------------------------------------------------------------------
                         P O R   P A C K E T
-------------------------------------------------------------------------
80000000
-------------------------------------------------------------------------

-------------------------------------------------------------------------------------------
                             C O M M A N D   P A C K E T
-------------------------------------------------------------------------------------------
            PARM4             PARM3             PARM2             PARM1             PARM0
045AFFFF 04580000 0456FFFF 04540000 0452FFFF 04500000 044EFFFF 044C0000 044AFFFF 04480000
-------------------------------------------------------------------------------------------
               SN            OPCODE
0446FFFE 04440001 04427F7F 04408080
-------------------------------------------------------------------------------------------


-------------------------------------------------------------------------------------------
                             C O M M A N D   P A C K E T
-------------------------------------------------------------------------------------------
            PARM4             PARM3             PARM2             PARM1             PARM0
045AFFFF 04580000 0456FFFF 04540000 0452FFFF 04500000 044EFFFF 044C0000 044AFFFF 04480000
-------------------------------------------------------------------------------------------
               SN            OPCODE
0446FFFD 04440002 04427F7F 04408080
-------------------------------------------------------------------------------------------


-------------------------------------------------------------------------------------------
                             C O M M A N D   P A C K E T
-------------------------------------------------------------------------------------------
            PARM4             PARM3             PARM2             PARM1             PARM0
045AFFFF 04580000 0456FFFF 04540000 0452FFFF 04500000 044EFFFF 044C0000 044AFFFF 04480000
-------------------------------------------------------------------------------------------
               SN            OPCODE
0446FFFC 04440003 04427F7F 04408080
-------------------------------------------------------------------------------------------


Ver 01.09  Thu Nov 16 19:20:30 2000    "(1) DCE is in Boot State"

Ver 01.09  Thu Nov 16 19:20:30 2000    "(2) Beginning 9-second wait..."
```

```
--------------------------------------------------------------------------------
                            C O M M A N D   P A C K E T
--------------------------------------------------------------------------------
            PARM4             PARM3             PARM2             PARM1             PARM0
045AFFFF 04580000 0456FFFF 04540000 0452FFFF 04500000 044EFFFF 044C0000 044AFFFF 04480000
--------------------------------------------------------------------------------
               SN            OPCODE
0446FFFB 04440004 04420C0C 0440F3F3
--------------------------------------------------------------------------------


--------------------------------------------------------------------------------
                            C O M M A N D   P A C K E T
--------------------------------------------------------------------------------
            PARM4             PARM3             PARM2             PARM1             PARM0
045AFFFF 04580000 0456FFFF 04540000 0452FFFF 04500000 044EFFFF 044C0000 044AFFFF 04480000
--------------------------------------------------------------------------------
               SN            OPCODE
0446FFFA 04440005 04427F7F 04408080
--------------------------------------------------------------------------------


--------------------------------------------------------------------------------
                            C O M M A N D   P A C K E T
--------------------------------------------------------------------------------
            PARM4             PARM3             PARM2             PARM1             PARM0
045AFFFF 04580000 0456FFFF 04540000 0452FFFF 04500000 044EFFFF 044C0000 044AFFFF 04480000
--------------------------------------------------------------------------------
               SN            OPCODE
0446FFF9 04440006 04427F7F 04408080
--------------------------------------------------------------------------------


--------------------------------------------------------------------------------
                            C O M M A N D   P A C K E T
--------------------------------------------------------------------------------
            PARM4             PARM3             PARM2             PARM1             PARM0
045AFFFF 04580000 0456FFFF 04540000 0452FFFF 04500000 044EFFFF 044C0000 044AFFFF 04480000
--------------------------------------------------------------------------------
               SN            OPCODE
0446FFF8 04440007 04427F7F 04408080
--------------------------------------------------------------------------------


--------------------------------------------------------------------------------
                            C O M M A N D   P A C K E T
--------------------------------------------------------------------------------
            PARM4             PARM3             PARM2             PARM1             PARM0
045AFFFF 04580000 0456FFFF 04540000 0452FFFF 04500000 044EFFFF 044C0000 044AFFFF 04480000
--------------------------------------------------------------------------------
               SN            OPCODE
0446FFF7 04440008 04427F7F 04408080
--------------------------------------------------------------------------------
```